

VER : 3A
PWA:
PWB:

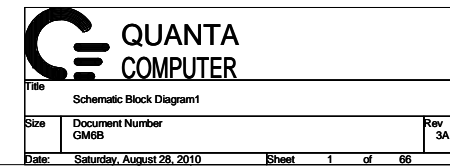



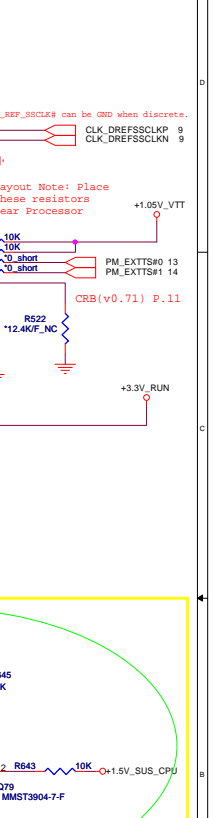
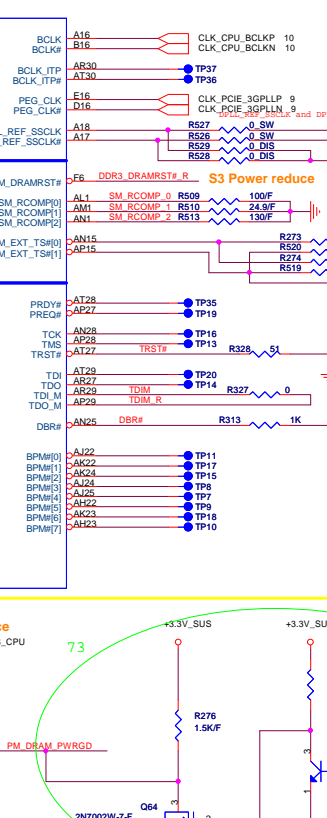
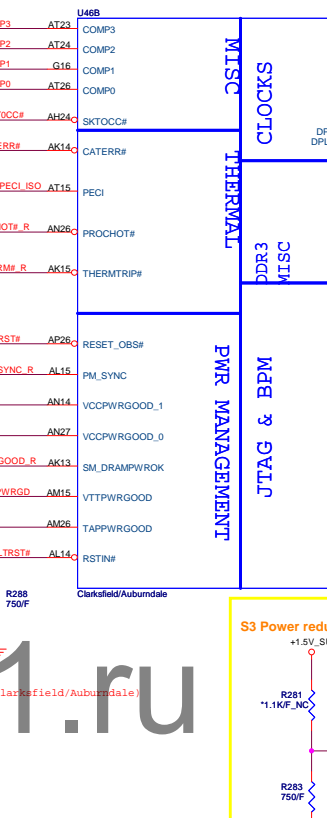
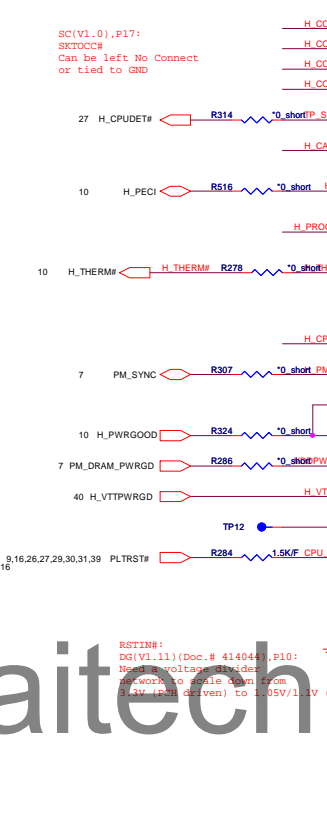
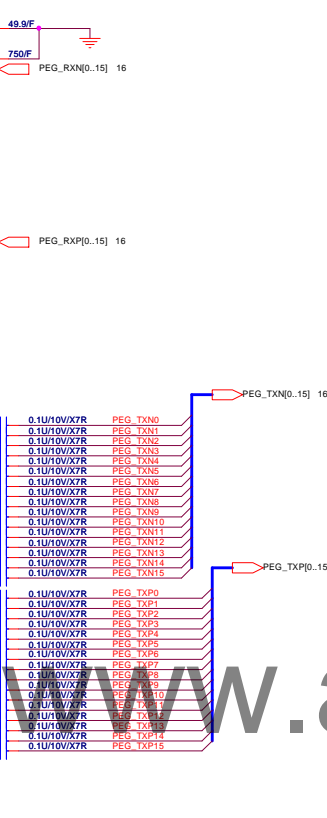
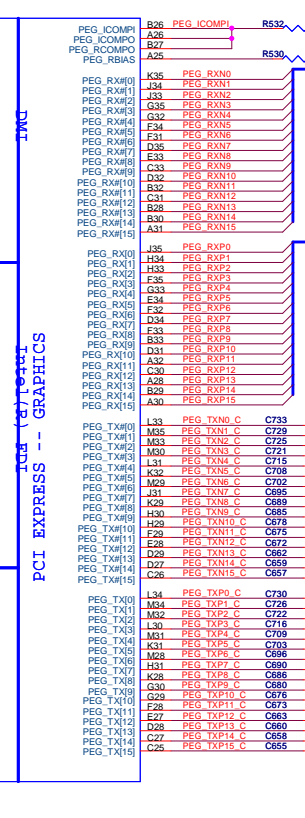
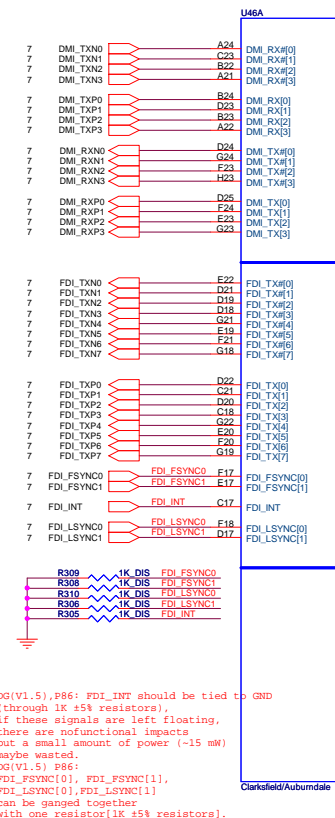
Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Clarksfield/Auburndale
7-12	PCH
13-14	DDRIII SO-DIMM(204P)
15	Clock Generator
16-22	N11P-GE
23	LCD CONN
24	HDMI CONN
25	MINI DP CONN
26	Card Reader (JMB389)
27	SIO (ITE8502)
28	FLASH / RTC
29	MINI-Card (WLANWPAN)
30	MINI-Card (WWAN)
31	LAN(RTL8111EL/RJ-45)
32	Right PUSB/ESATA
33	SATA (HDD & ODD)
34	TP / KEYBOARD
35	SWITCH / LED / T-Screen
36	FAN / THERMAL
37	Azelia CODEC
38	AUDIO AMP
39	Left USB/MMB CONN
40	System Reset Circuit
41	Charger (ISL88731)
42	CPU CORE(ADP3212)
43	1.5_DDR/0.75(RT8207A)
44	1.05V_VTT(VT358)
45	1.05V_PCH(VT356)
46	3V/5V (TPS51427A)
47	GFX_CORE(ADP3211)
48	1.8V_RUN(HPA00835RTER)
49	VGA_N11P-dGFX(MAX17007)
50	Run Power Switch
51	DCin & Batt
52	PAD & SCREW
53	SMBUS BLOCK
54	THERMAL MAP
55	Power Block Diagram
56	Power sequence Block
57	
58	
59	
60	

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

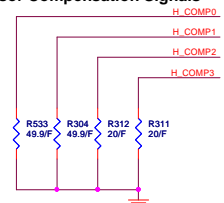


DG(V1.5),P86: FDI_INT should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nonfunctional impacts but a small amount of power (~15 mW) maybe wasted.

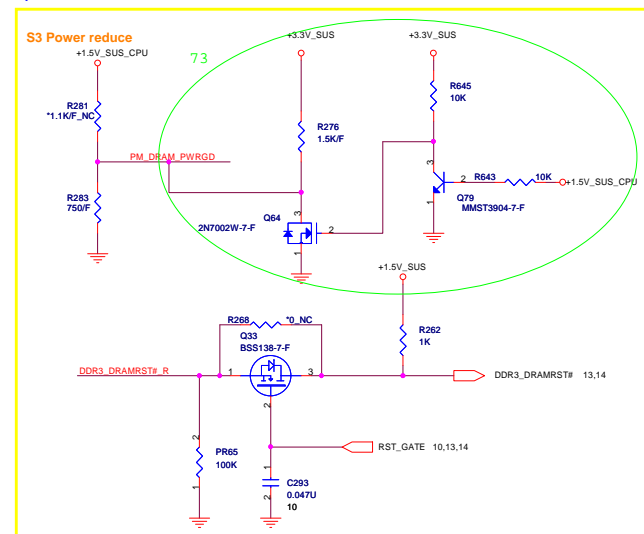
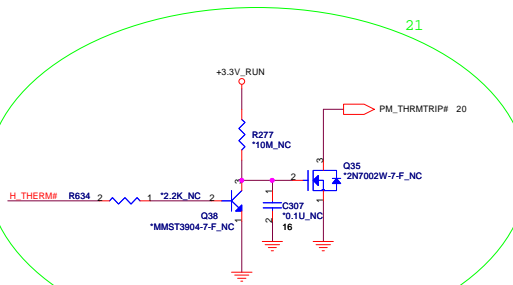
DG(V1.5) P86: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor[1K ±5% resistors].

Clarksfield/Auburndale

Processor Compensation Signals



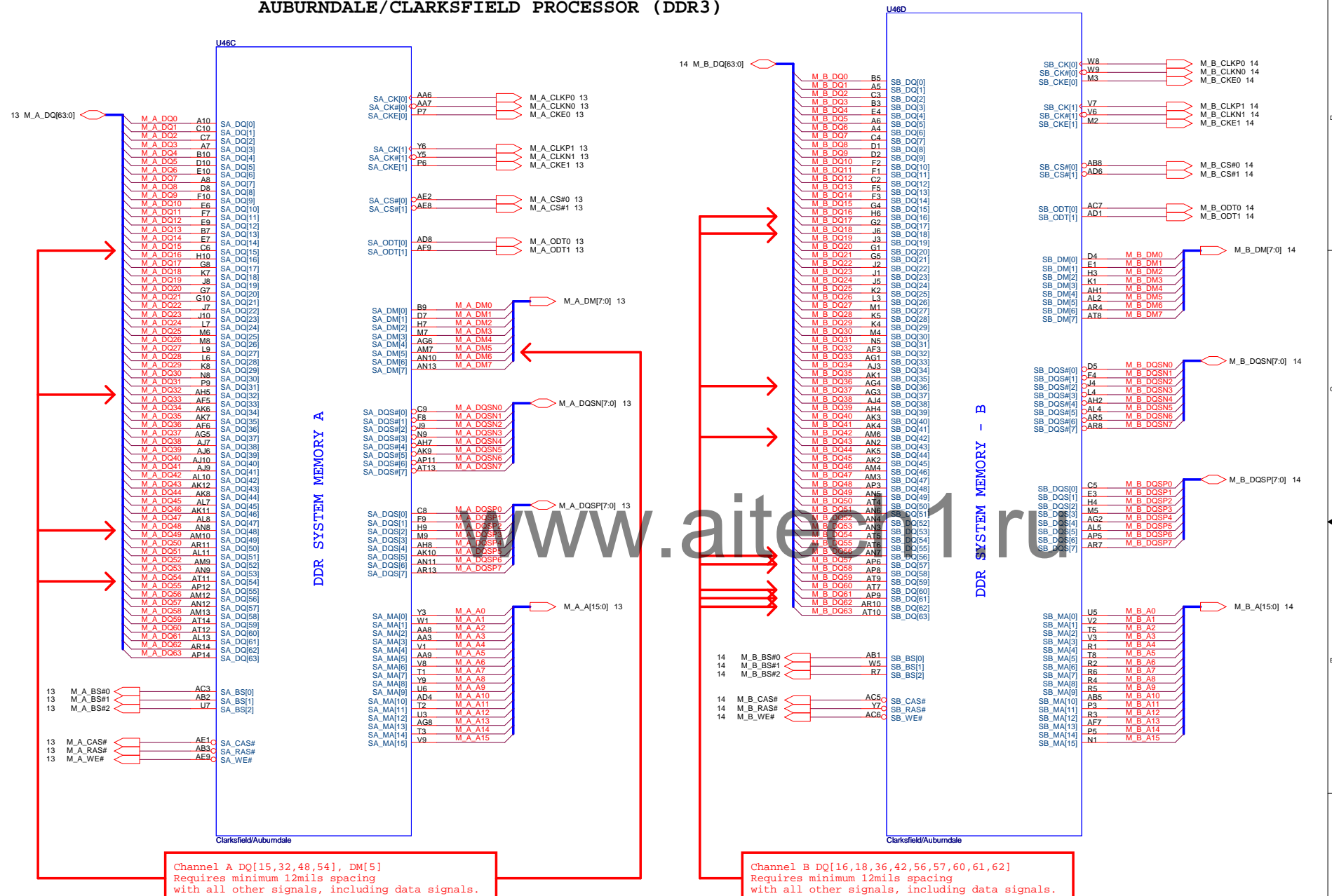
DG(V1.0),P17: COMP[0..1] 49.9-Ω ±1% pull-down to GND
COMP[2..3] 20-Ω ±1% pull-down to GND



QUANTA
COMPUTER

File: ARRD/CPD 1/4
Size: Document Number 6M6B
Date: Saturday, August 28, 2010
Sheet: 3 of 66
Rev: 3A

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

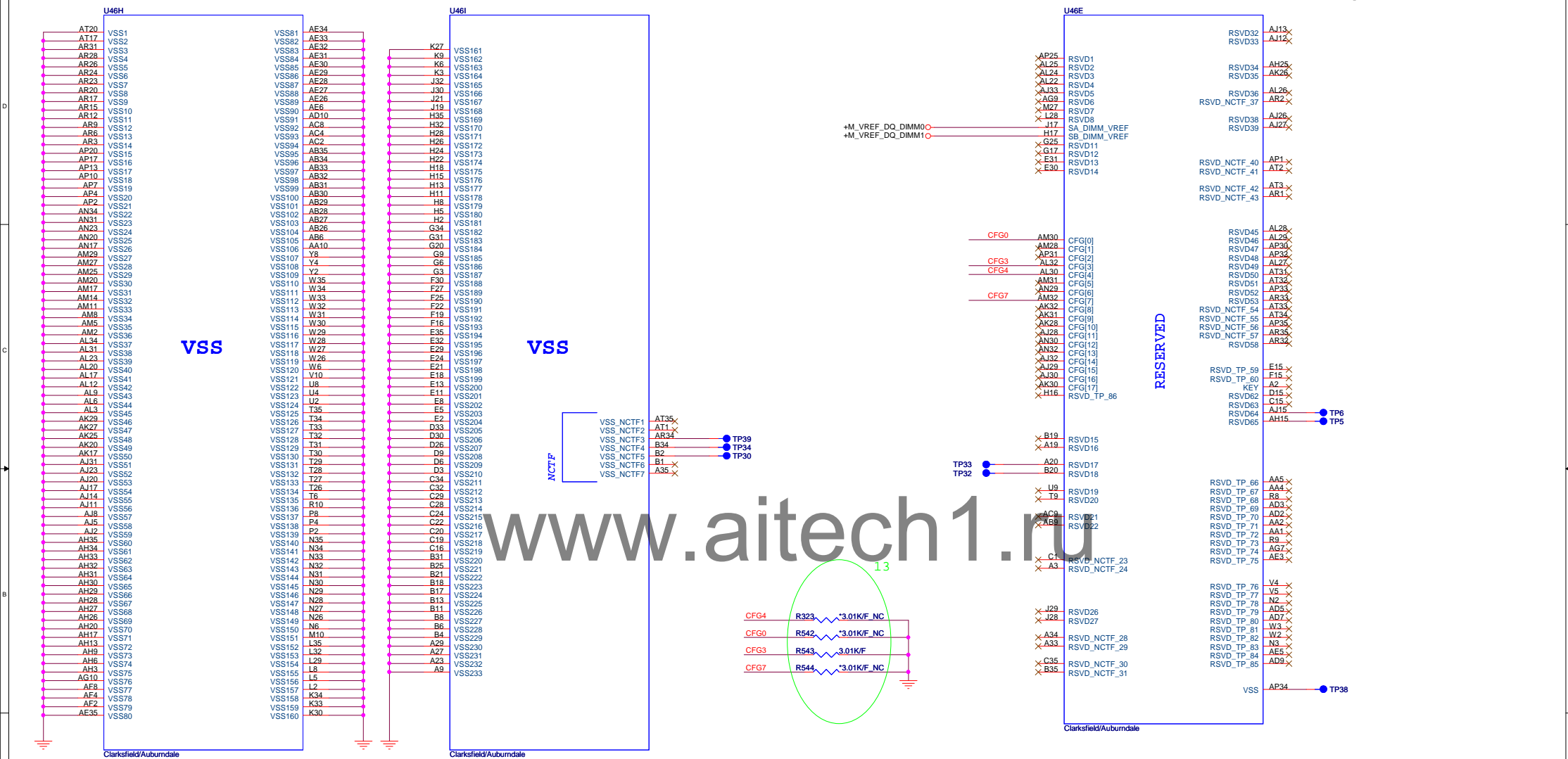


AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

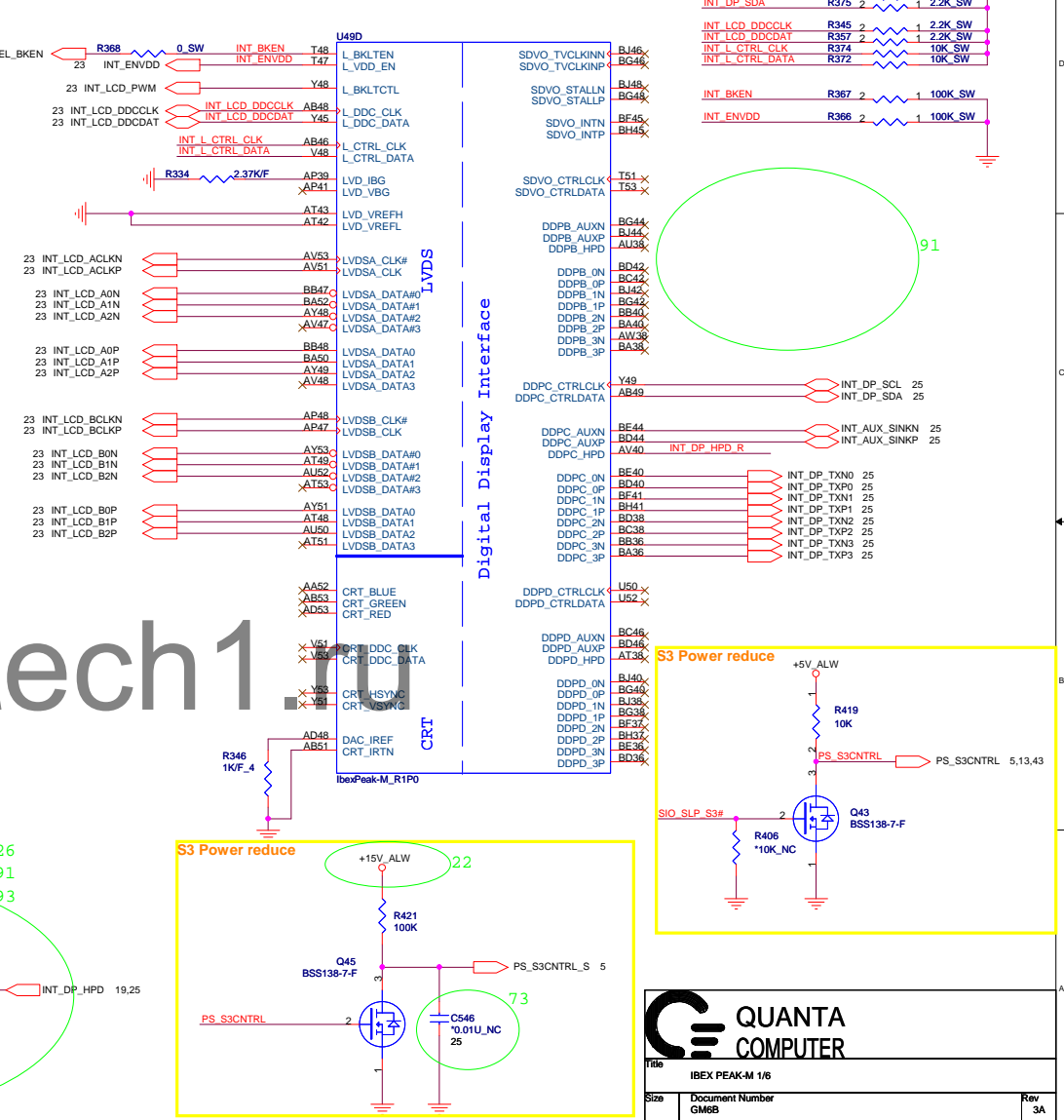
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

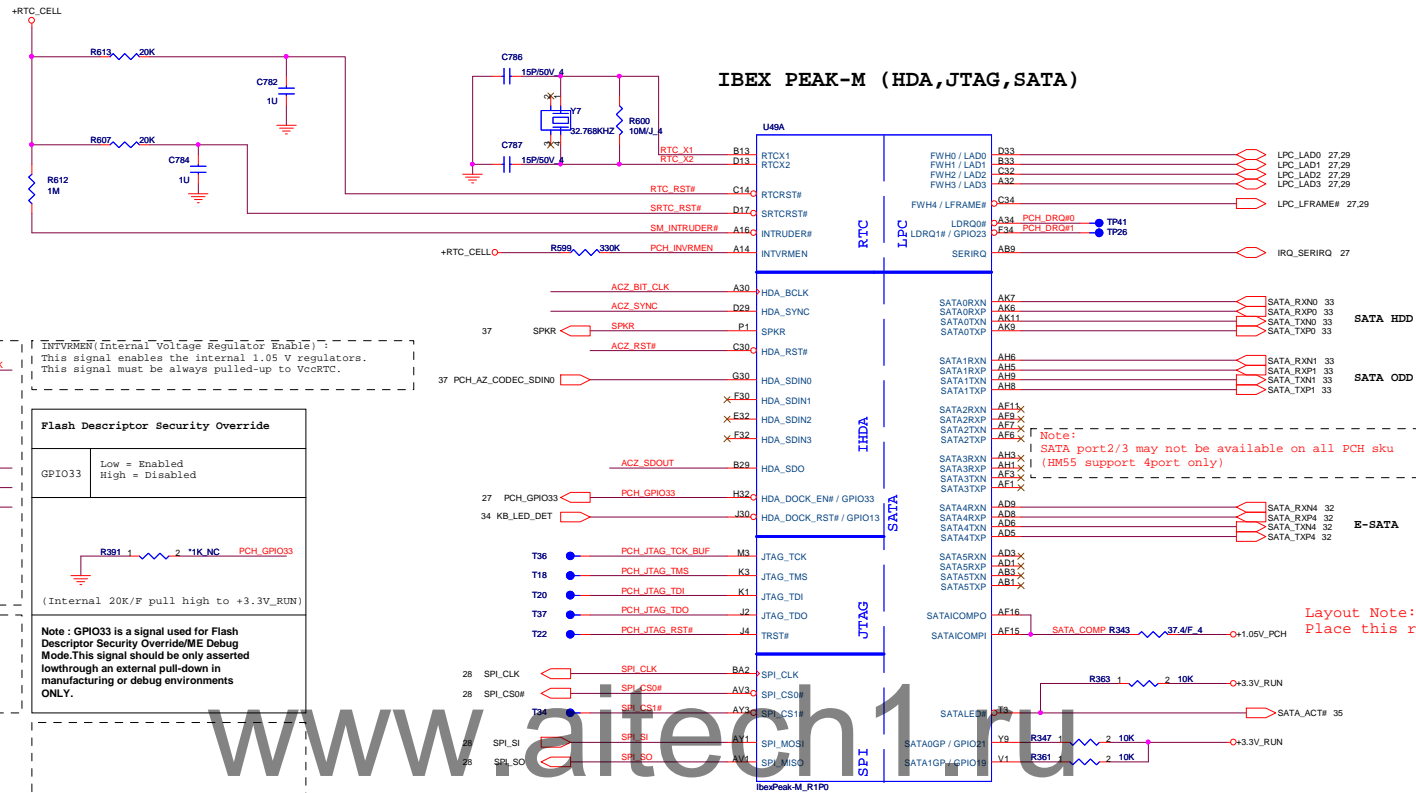
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

Title		
ARRD/CFD 4/4		
Size	Document Number	Rev
GM68		3A
Date:	Saturday, August 28, 2010	Sheet 6 of 66

IBEX PEAK-M (LVDS, DDI)



IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M 2/6

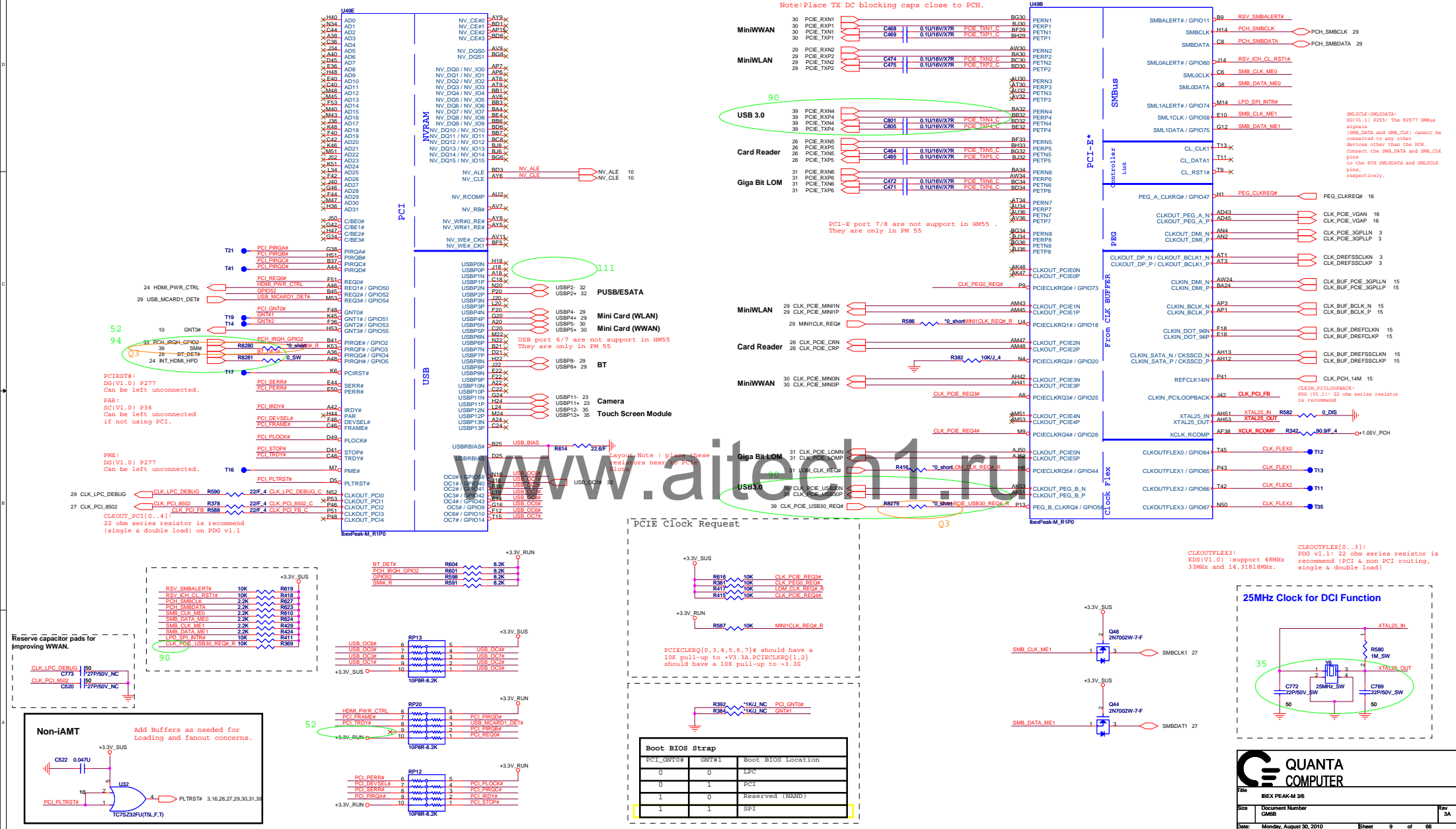
Document Number
GMB6

Date: Saturday, August 28, 2010

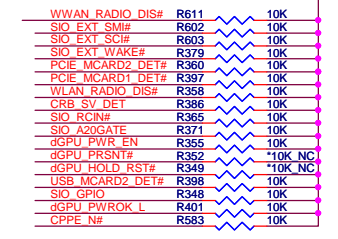
Sheet 6 of 66

Rev 3A

IBEX PEAK-M (PCI-E,SMBUS,CLK)



FFS INT2	R638	10K
RSV WOL EN	R618	10K
TS EN	R393	10K
LAN PHY PWR CTRL	R413	10K
TEST WOOFER EN	R370	1K
USB3 PWR EN	R414	10K
RST GATE	R395	10K

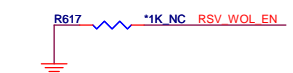
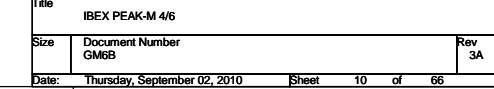


dGPU_PRSENT# R362 10K

dGPU always exist

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

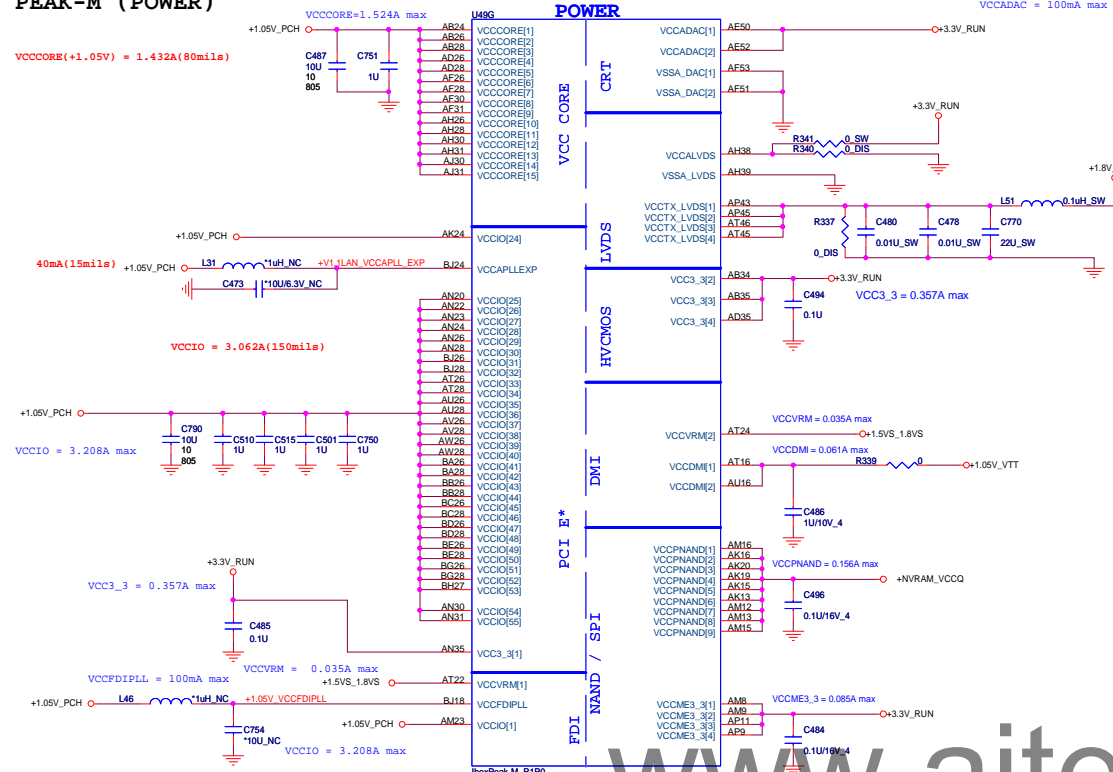
```
BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.
```



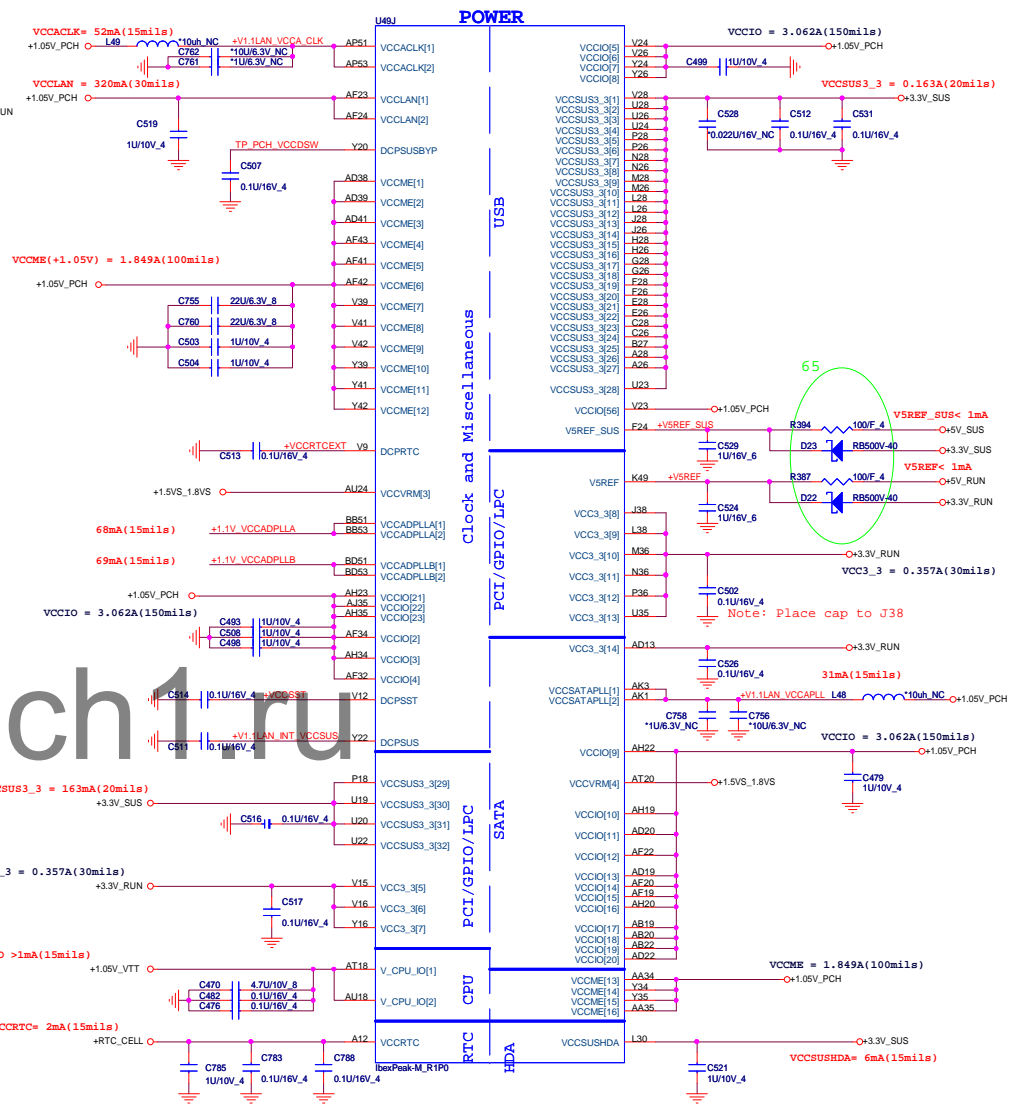
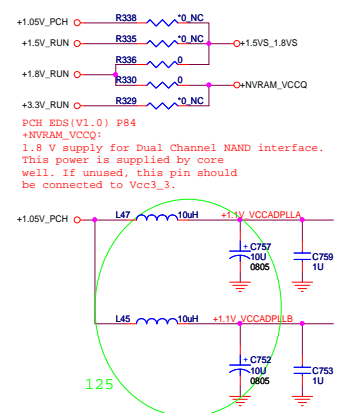
Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high

SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

IBEX PEAK-M (POWER)

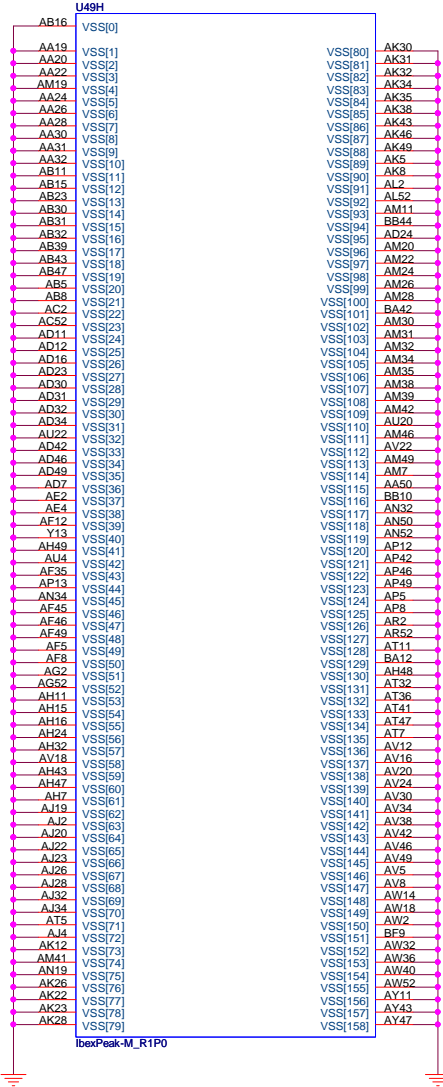


VCCME3_3:
ESD(V1.0)P84:supply for the Intel Management Engine,This is a separate power plane
that may or may not be powered in S3-S5 states.
This plane must be on in S0
and other times the Intel Management Engine is used.

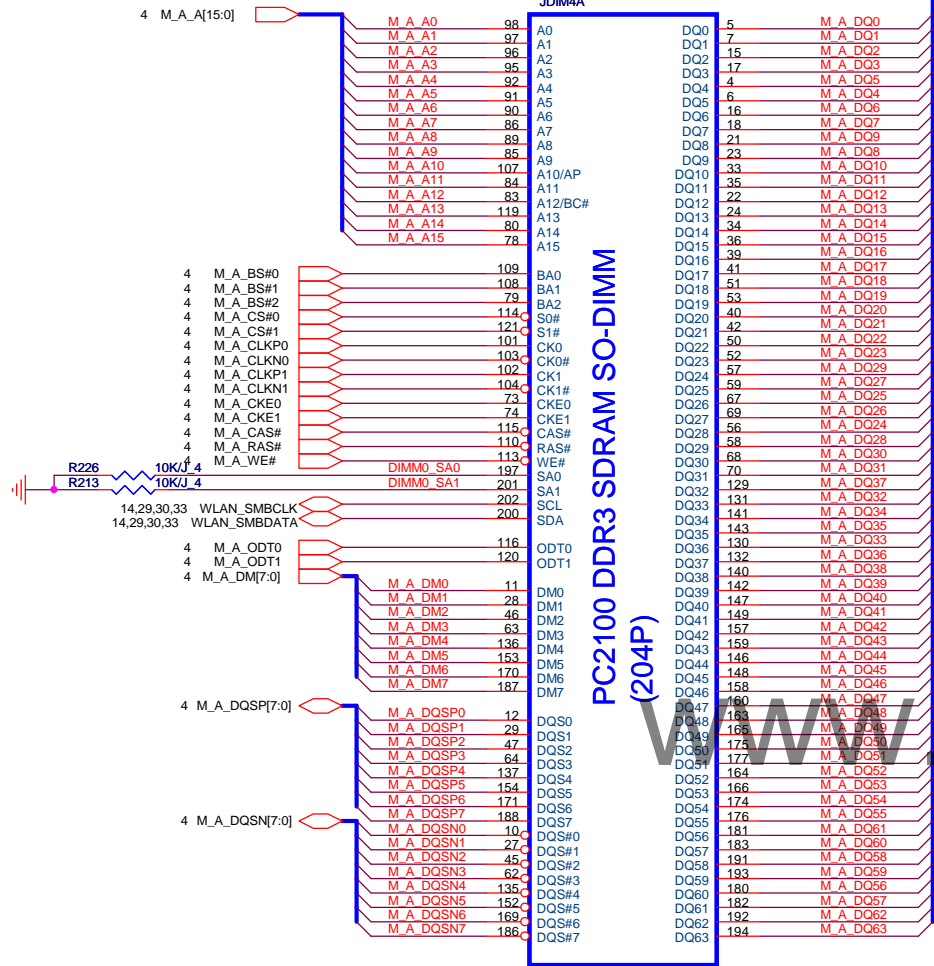


Title				IBEX PEAK-M 5/6			
Size	Document Number						Rev
	GM6B						3A
Date:	Saturday, August 28, 2010			Sheet	11	of	66

IBEX PEAK-M (GND)

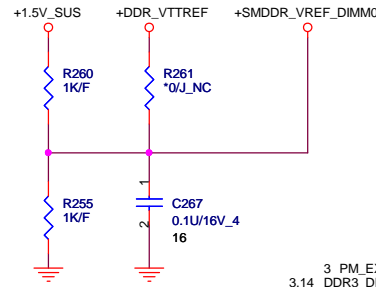
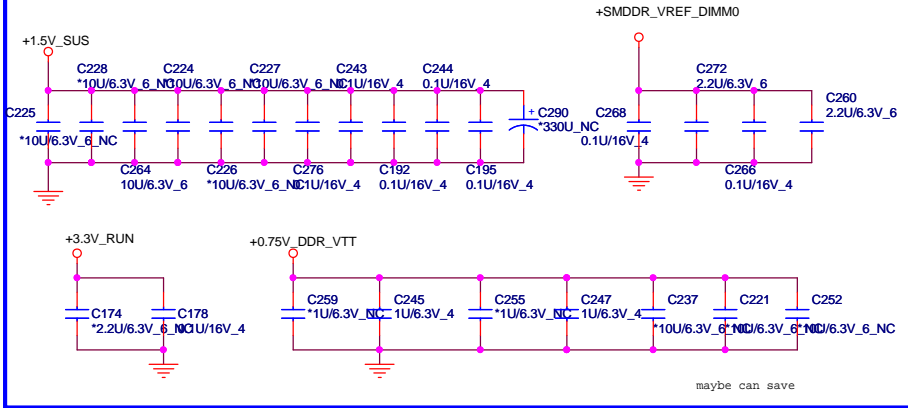


Title			IBEX PEAK-M 6/6
Size	Document Number	Rev	
GM6B		3A	
Date:	Saturday, August 28, 2010	Sheet	12 of 66

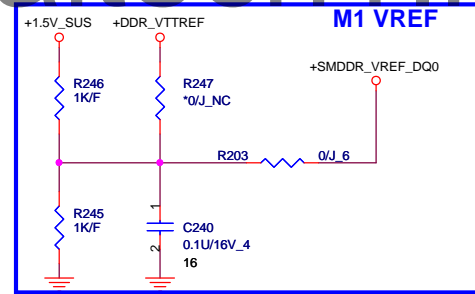


TYC_1932210-1

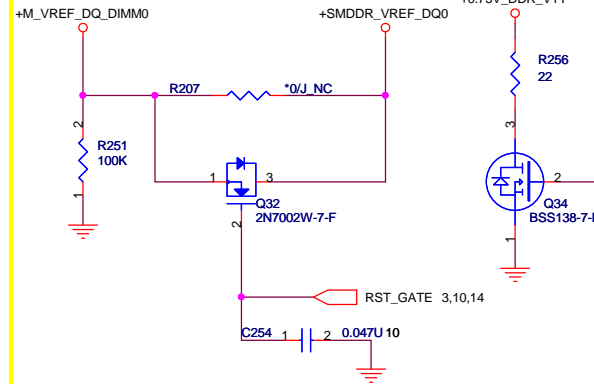
Place these Caps near So-Dimm0.



2.48A



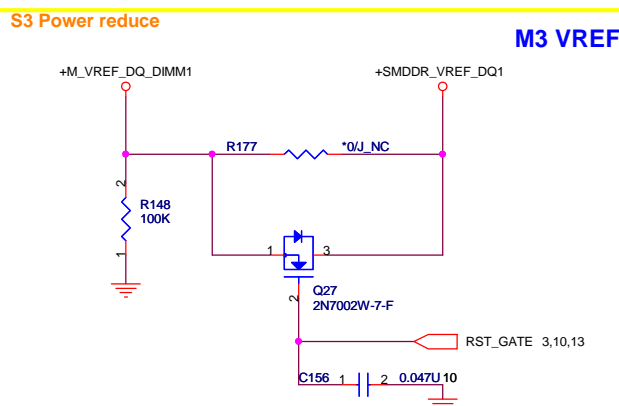
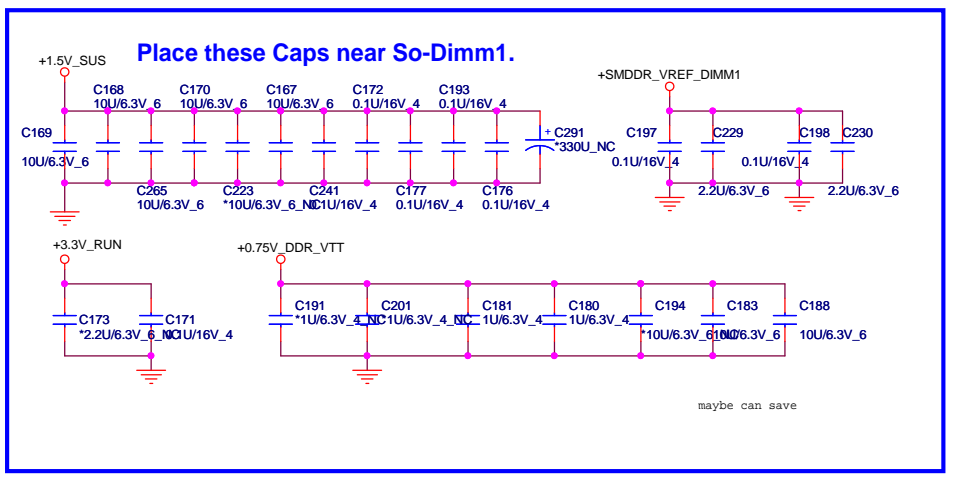
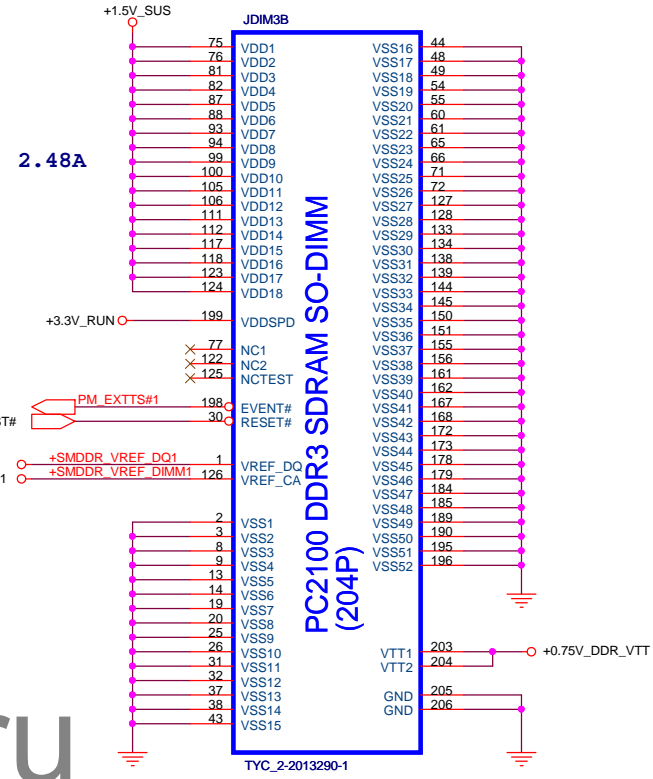
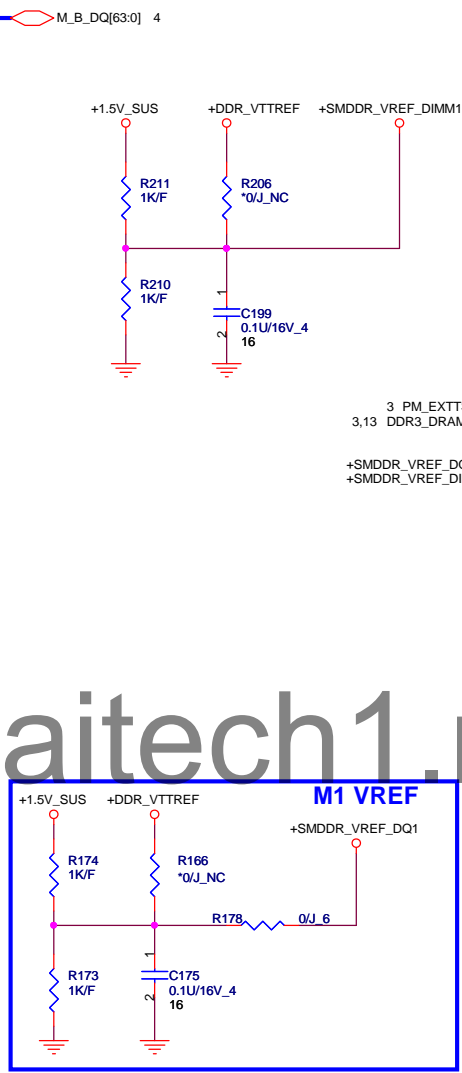
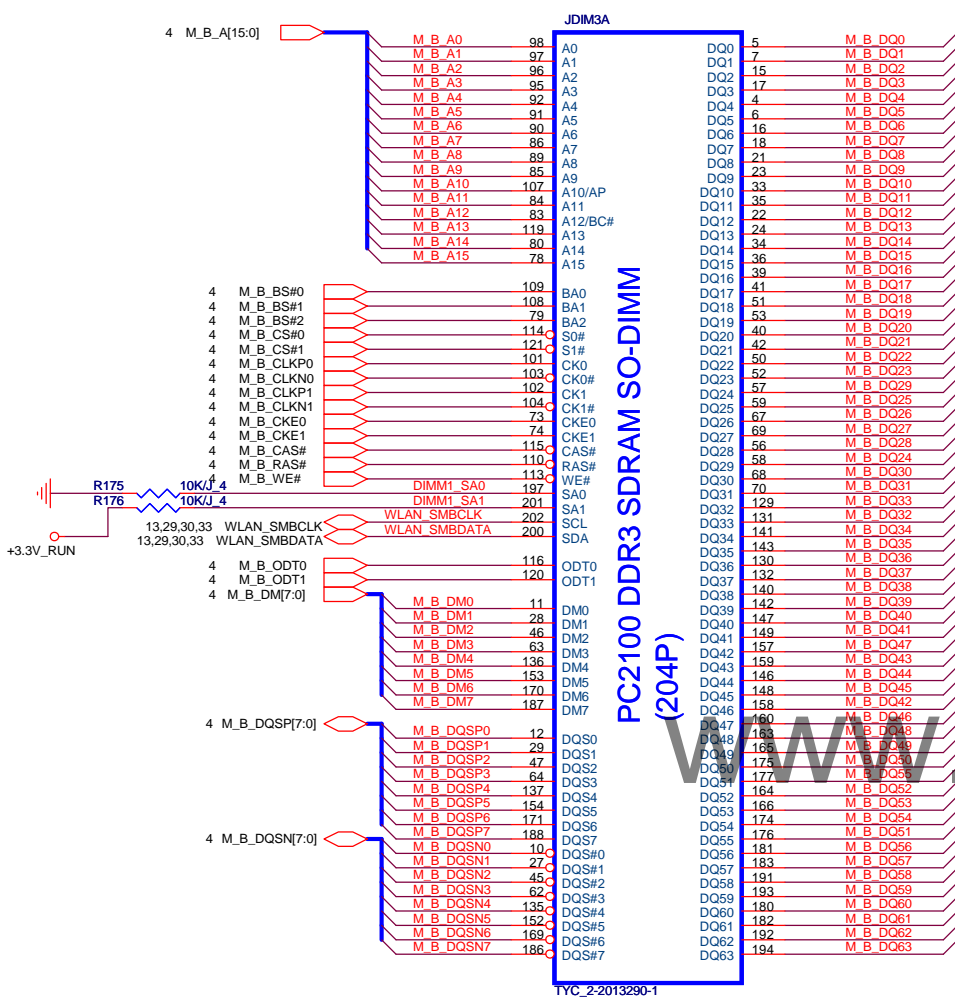
S3 Power reduce



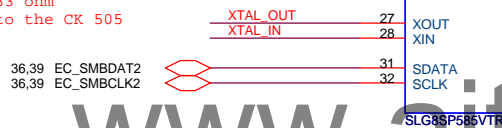
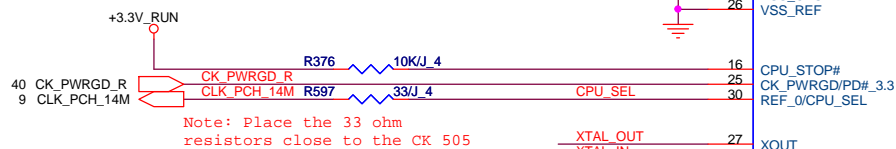
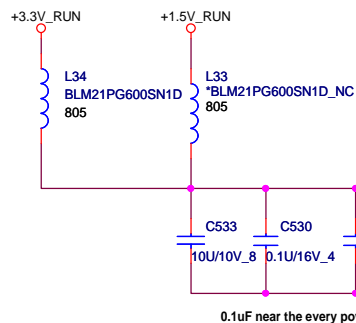
M3 VREF

VREF_DQ	R203	R207	R247 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X

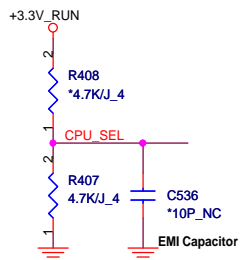
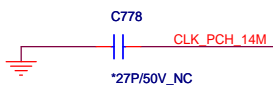




VREF_DQ	R178	R177	R166 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X



Add capacitor pads for improving WWAN.

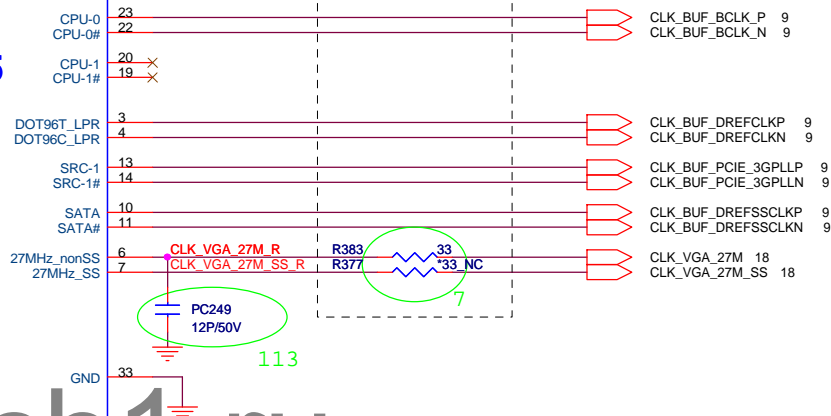


PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

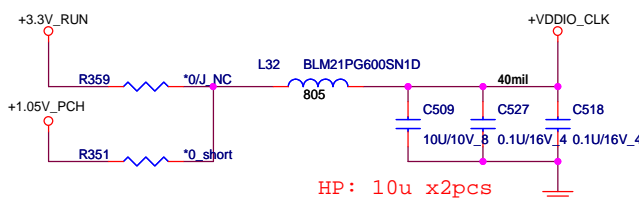
CPU_SEL:
 SLG date sheet (V0.2) P15:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.
 Realtek date sheet(V1.2) P11:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.
 IDT date sheet(V0.7) P10:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.

**CK505
QFN32**

Place within 0.5" of CLKGEN



Realtek: 0.1uFx3pcs, 22uFx1pcs
 IDT: 0.1uFx2pcs, 10uFx1pcs



SLG, IDT: +1.05V
 Realtek: +3.3V

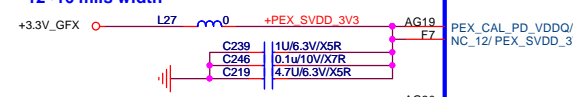
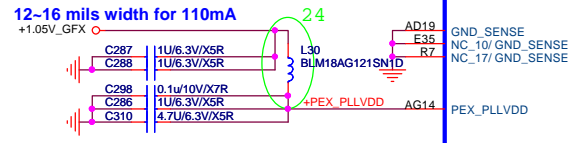
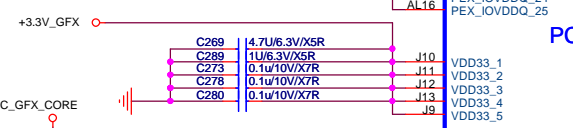
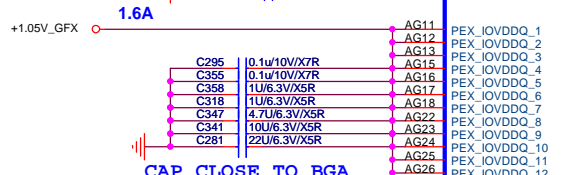
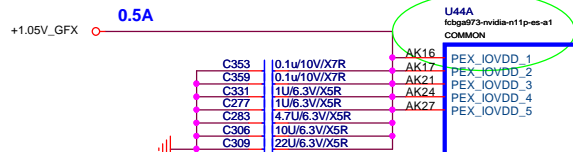
Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

+VDDIO_CLK:
 SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
 Realtek date sheet(V1.2) P11: Min 1.05V, Max 3.3V.
 IDT date sheet(V0.7) P10: Min 0.9975V, Max 3.465V.

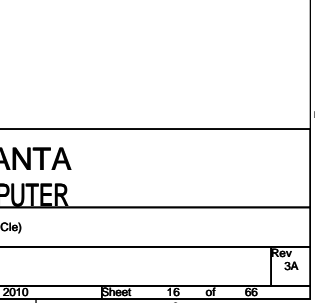
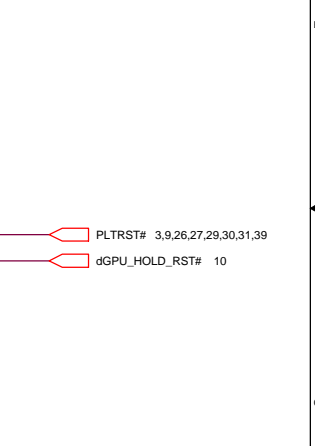
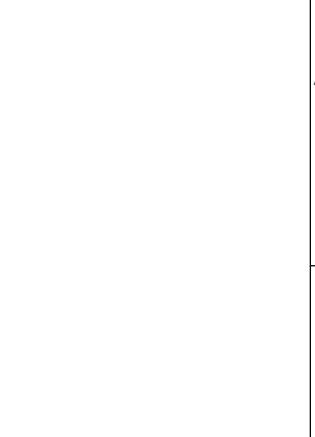
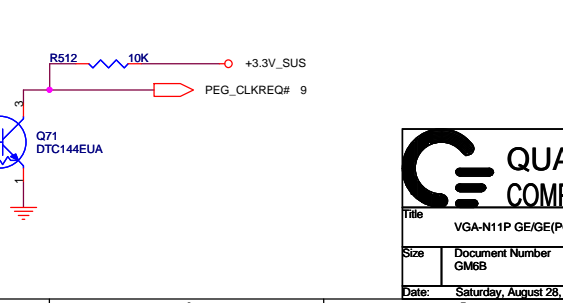
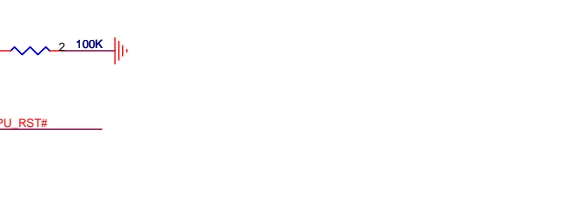
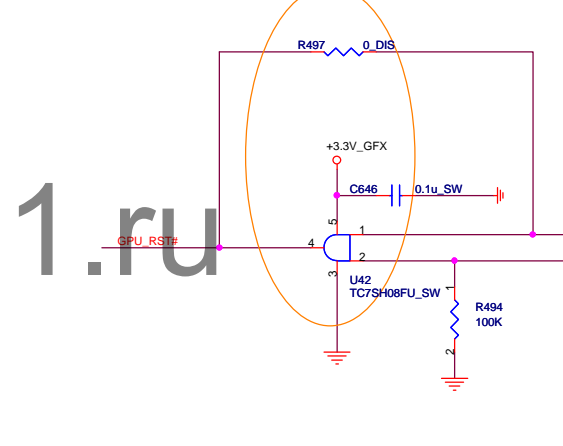
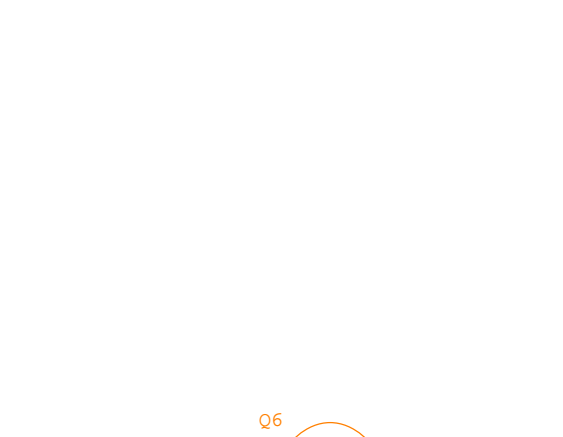
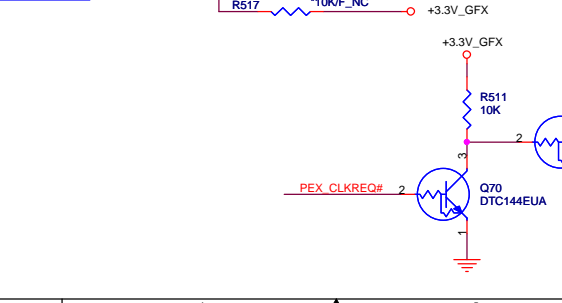
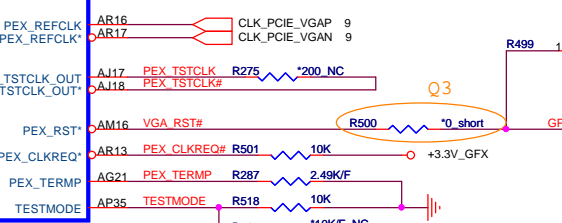
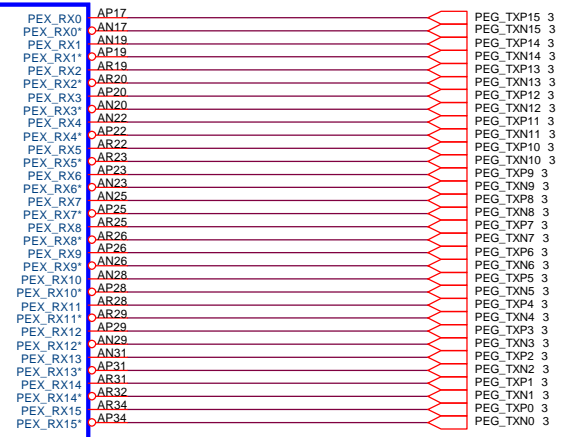


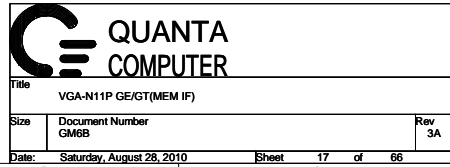
Title Clock Generator		
Size GM6B	Document Number	Rev 3A
Date: Saturday, August 28, 2010	Sheet 15	of 66

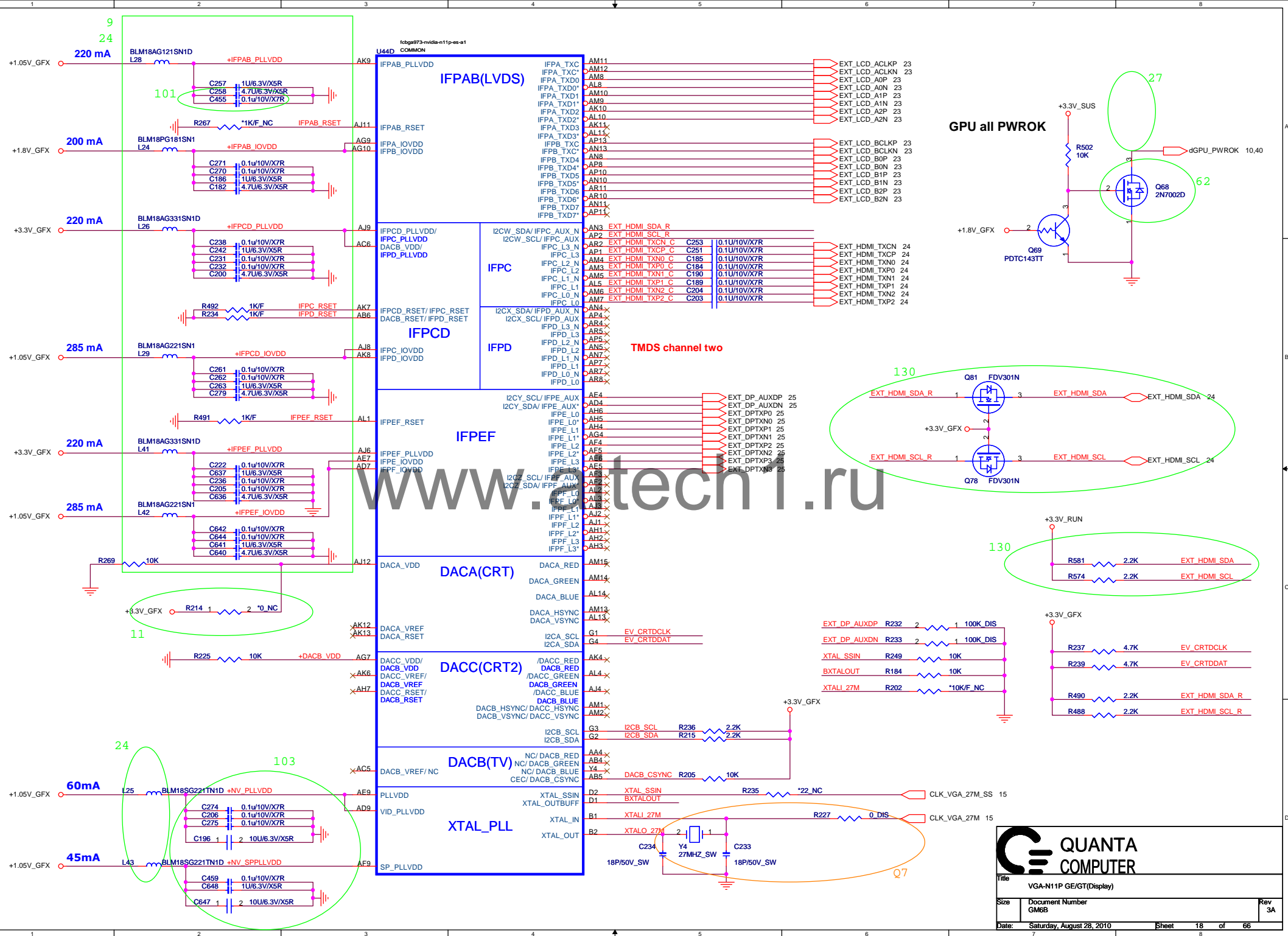
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

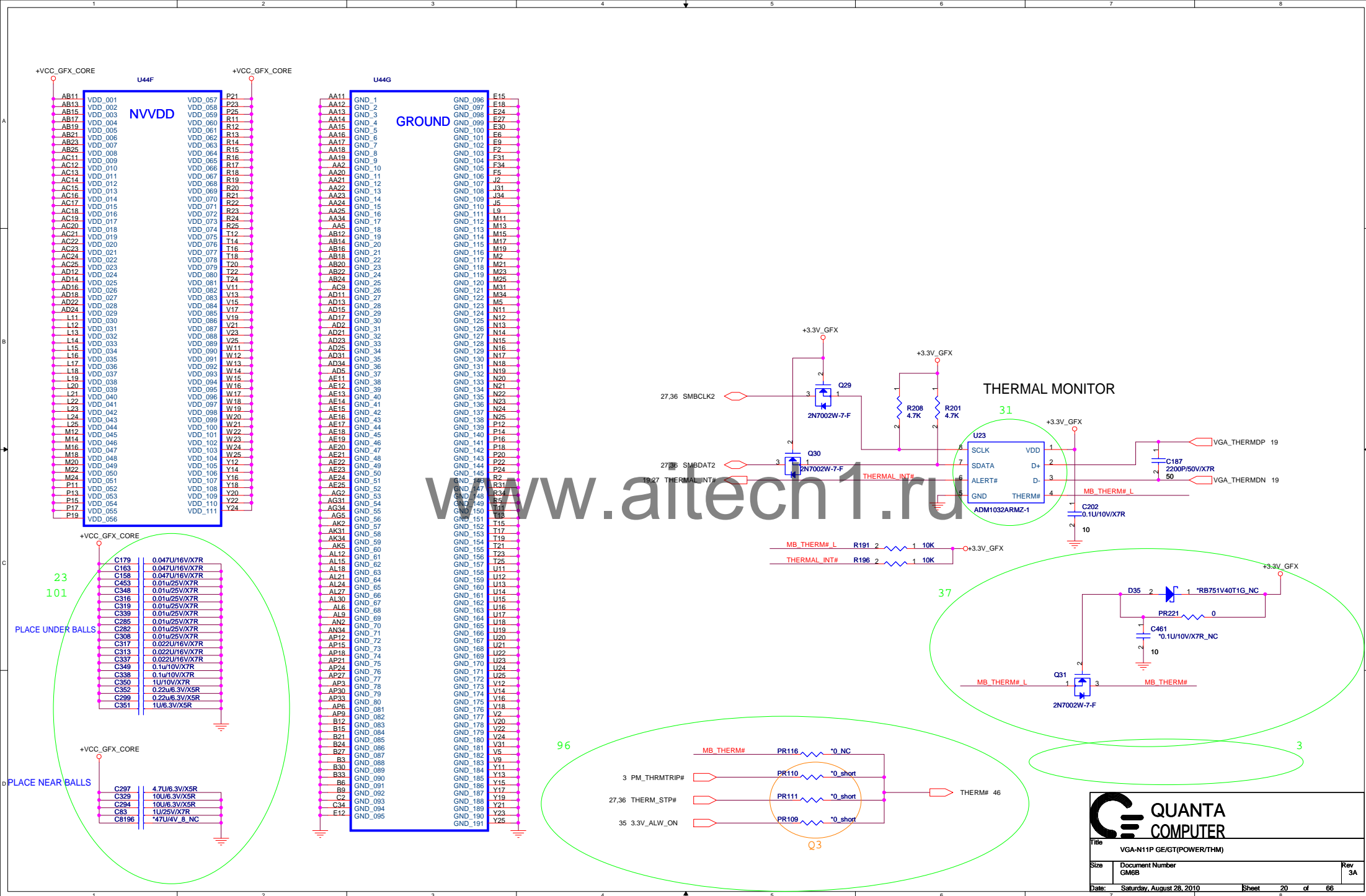


PCI EXPRESS





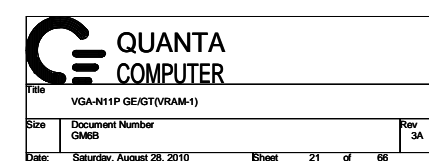




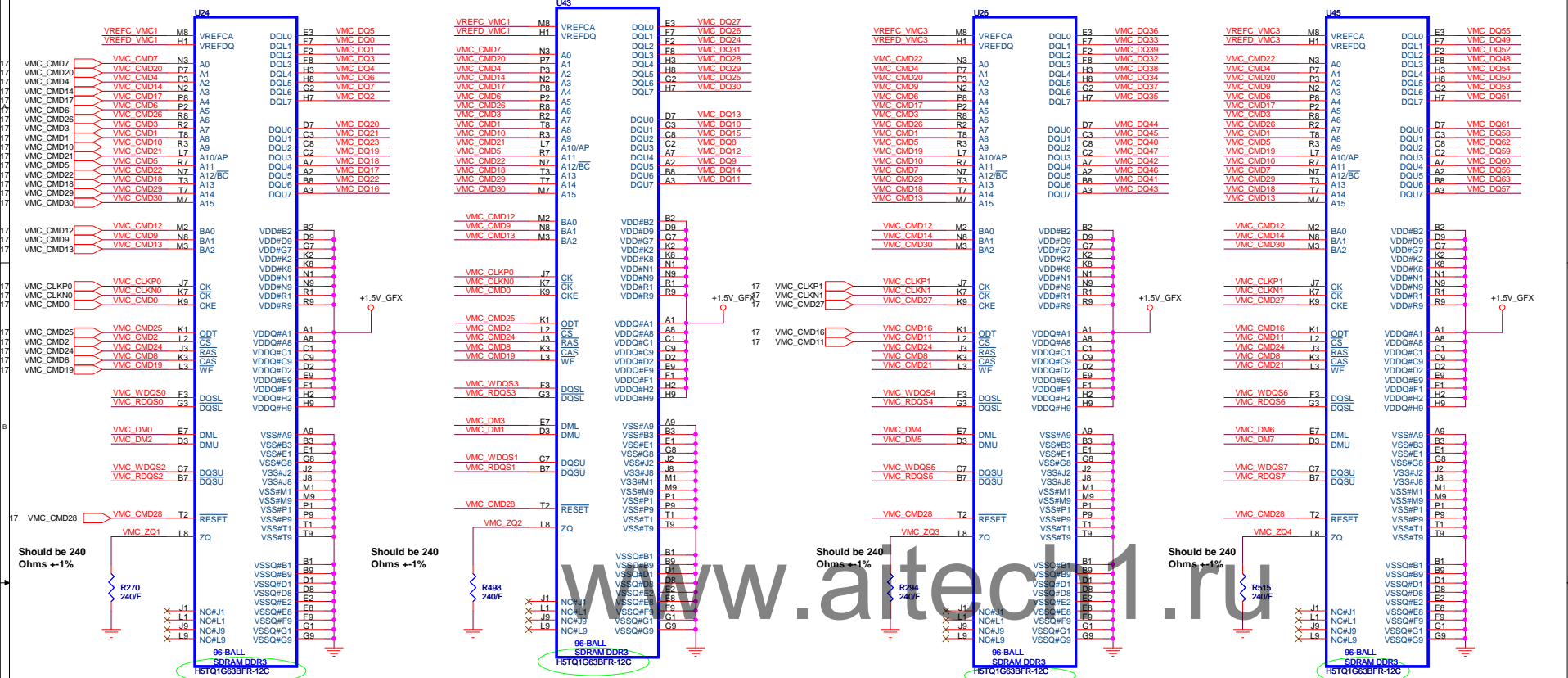

```

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

```



CHANNEL B: 512MB/1024MB DDR3

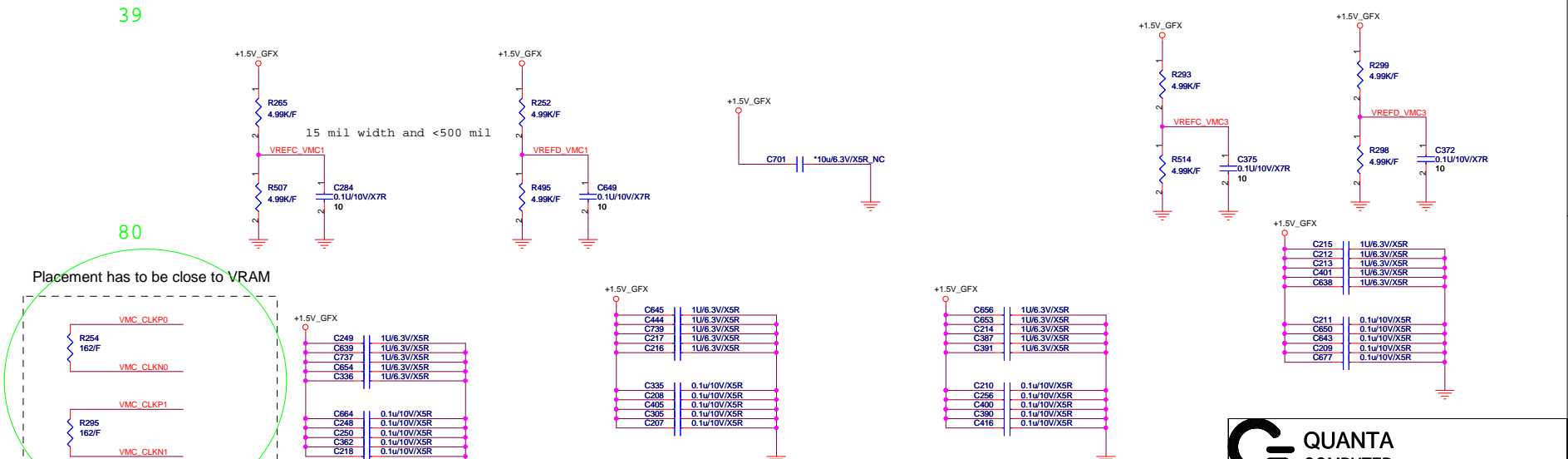


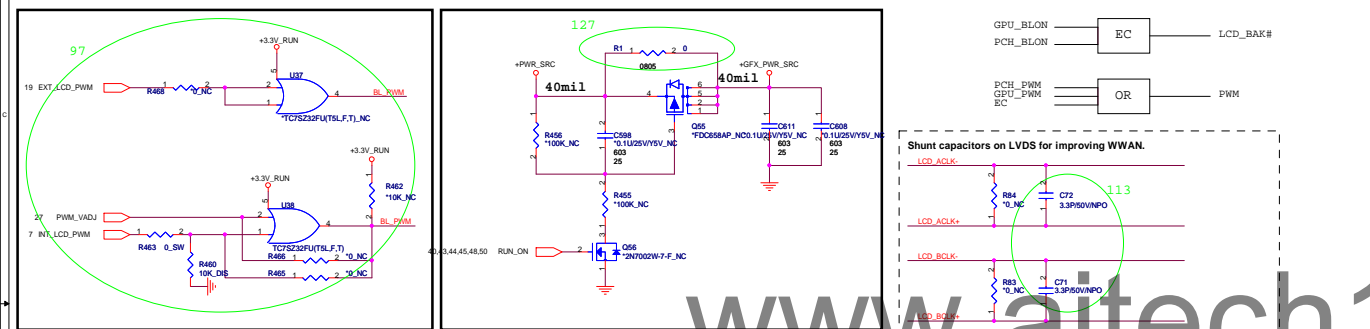
Should be 240 Ohms ±1%

R204 240F

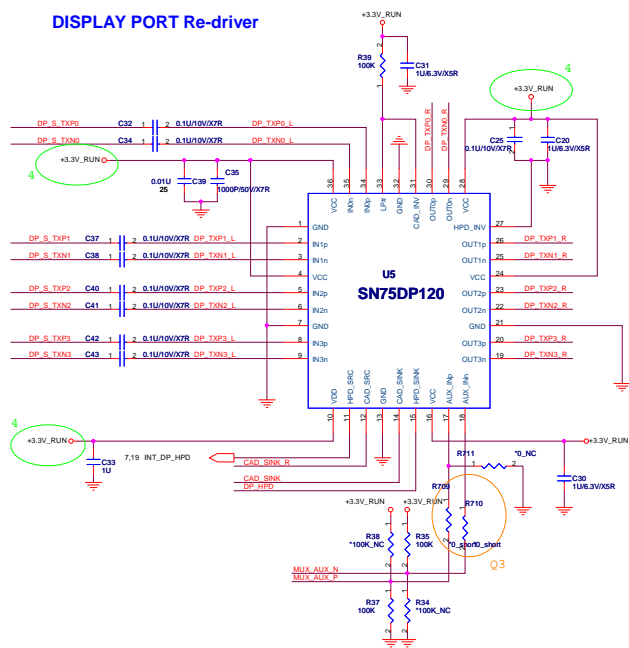
Should be 240 Ohms ±1%

R504 240F

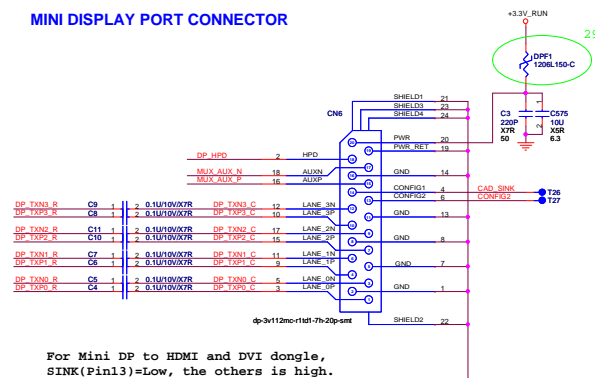




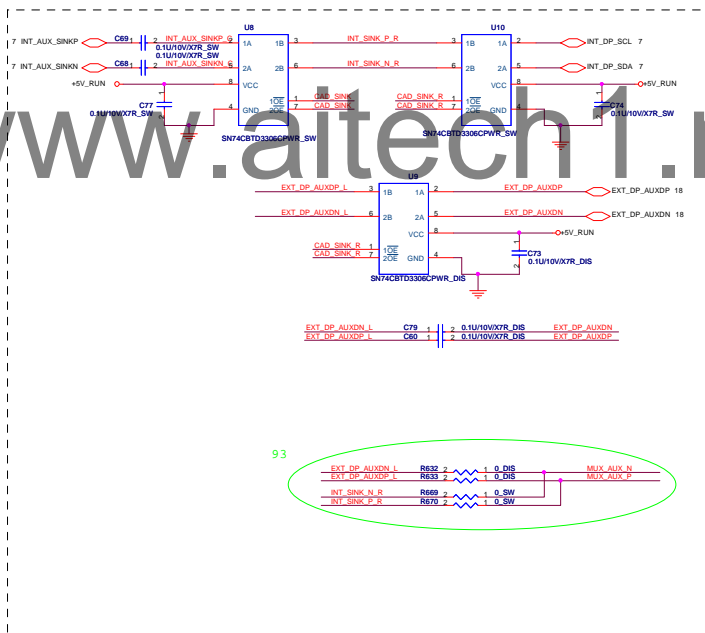
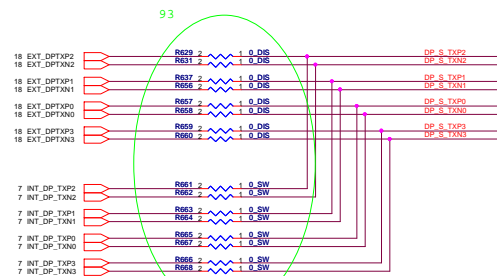
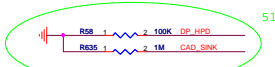
DISPLAY PORT Re-driver



MINI DISPLAY PORT CONNECTOR



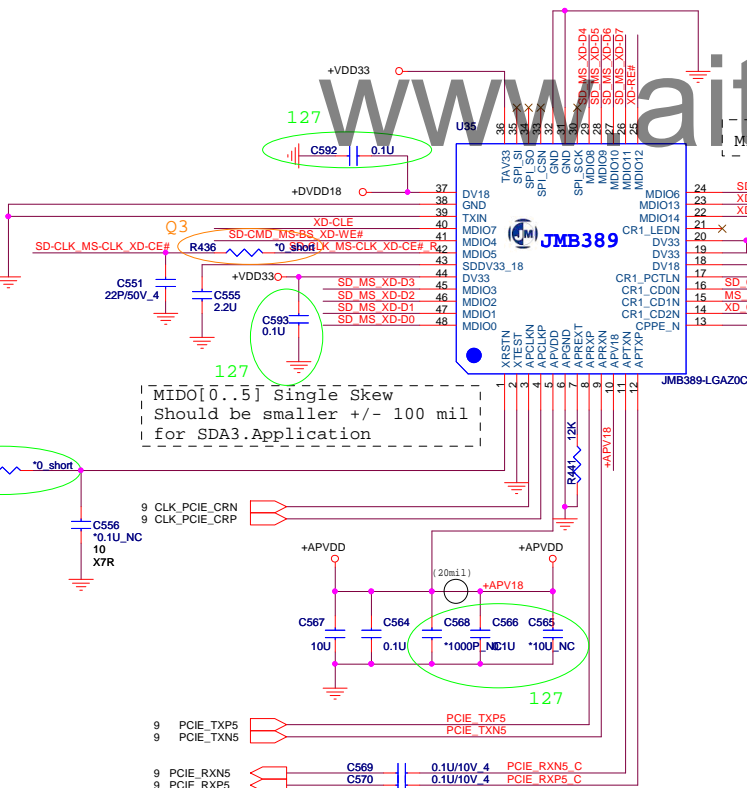
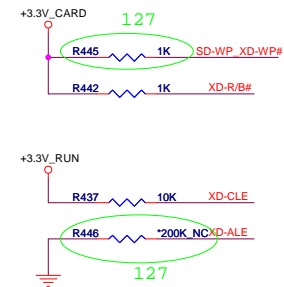
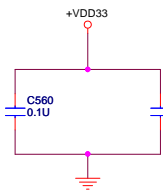
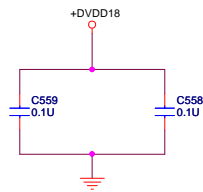
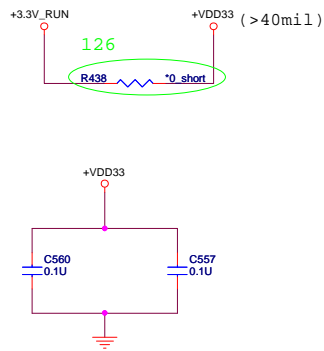
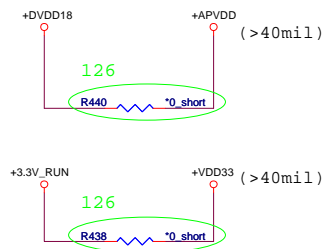
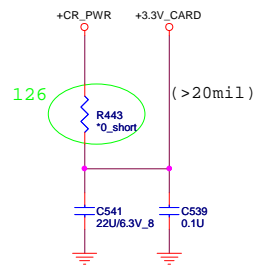
For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.



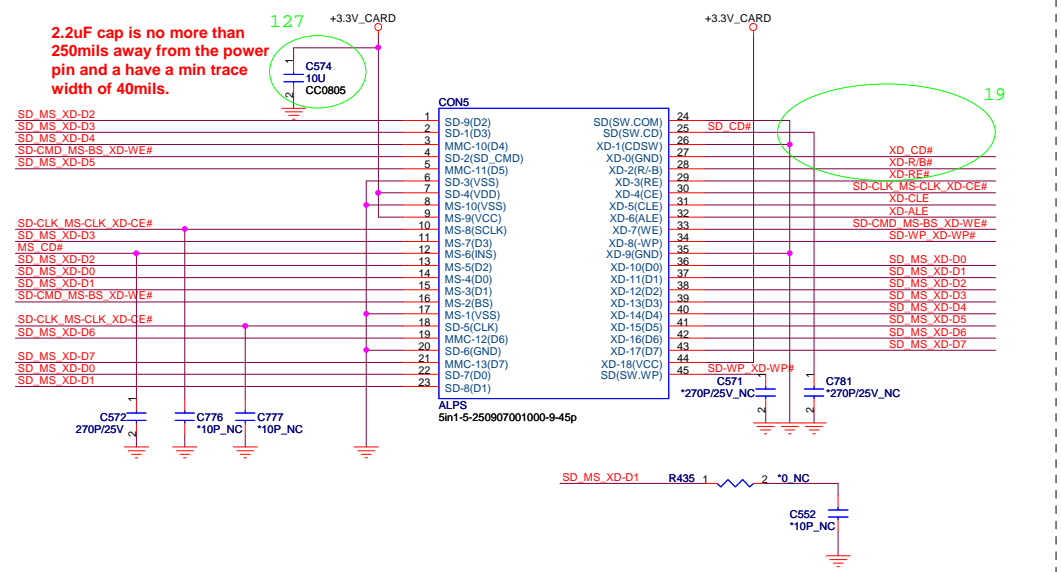
OE	Output
L	A=B
H	Z



Doc	Display Port CONN	Rev	3A
Size	Document Number	Class	
Date	Saturday, August 28, 2010	Sheet	25 of 66



MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3 Application



MIDO Single End = 50 ohm

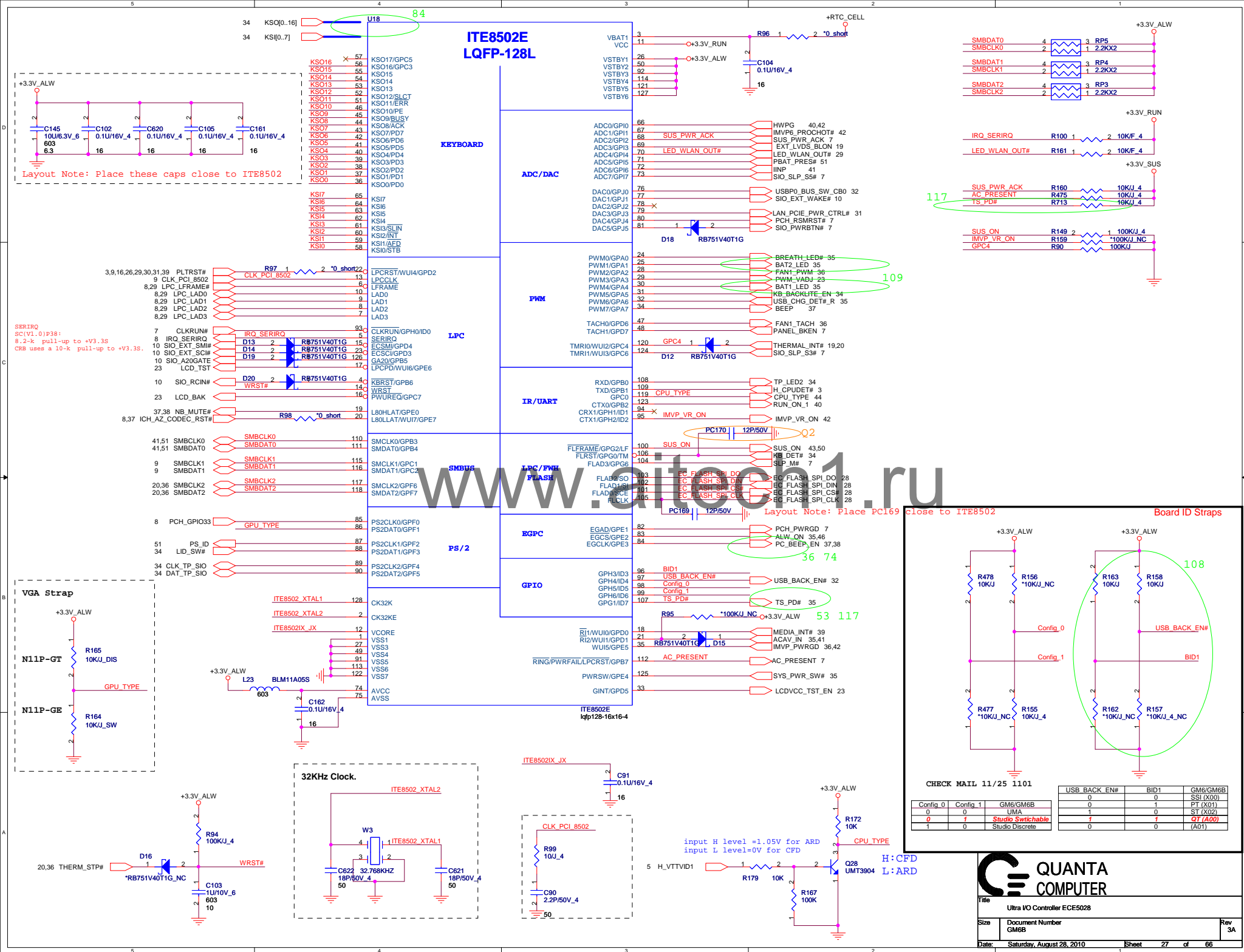
Needs close to Pin17: 12mil/<250mil

Layout Note:
Place this cap close to pin 18

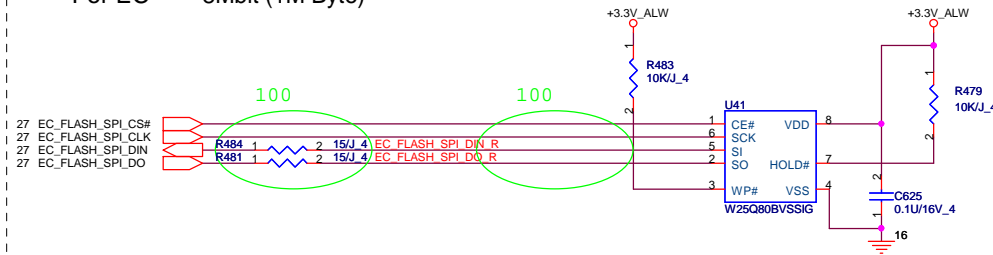
Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD / MMC / xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CS#
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_AL#
CR1_LEDN		SD_LEDN	MS_LEDN	XD_LEDN
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

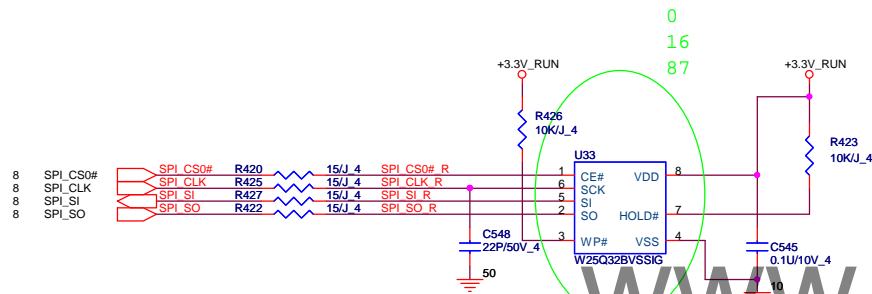




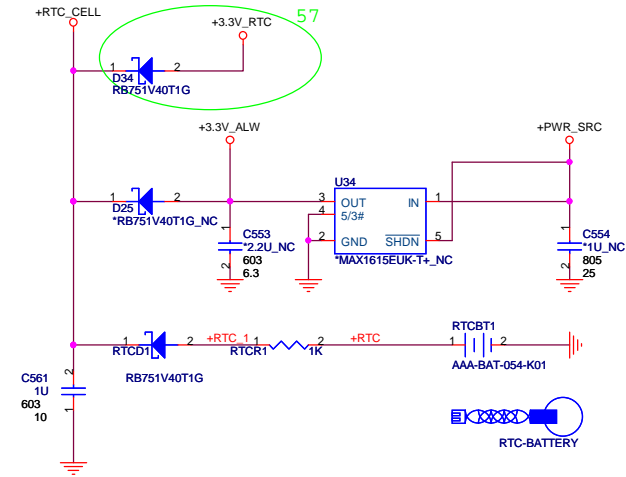
For EC 8Mbit (1M Byte)



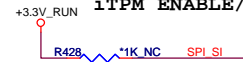
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE

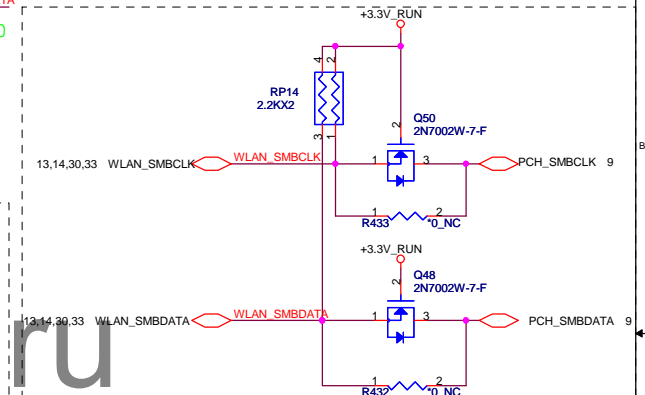
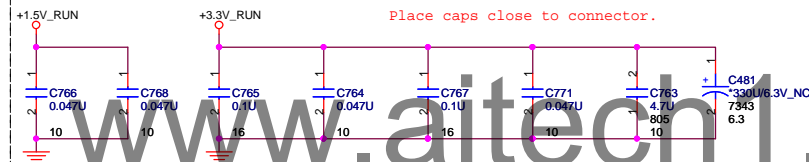
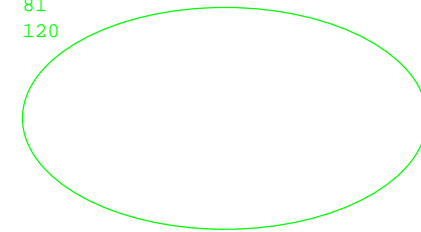


TPM Function	R428
Enable	Mount
Disable	NC (Default)

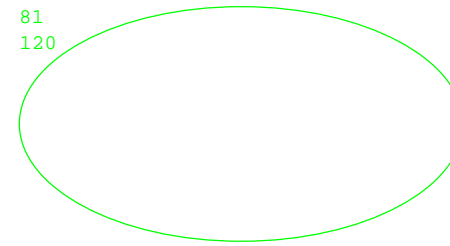


Title	FLASH/RTC		
Size	Document Number	Rev	
	GM6B	3A	
Date:	Saturday, August 28, 2010	Sheet	28 of 66

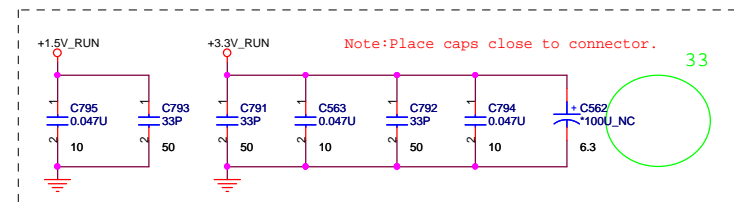
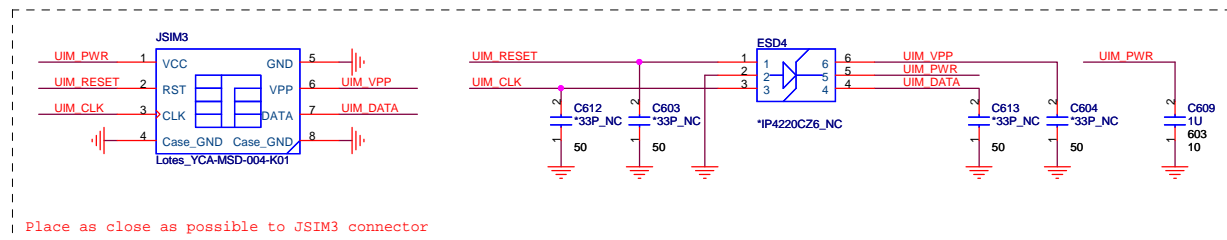
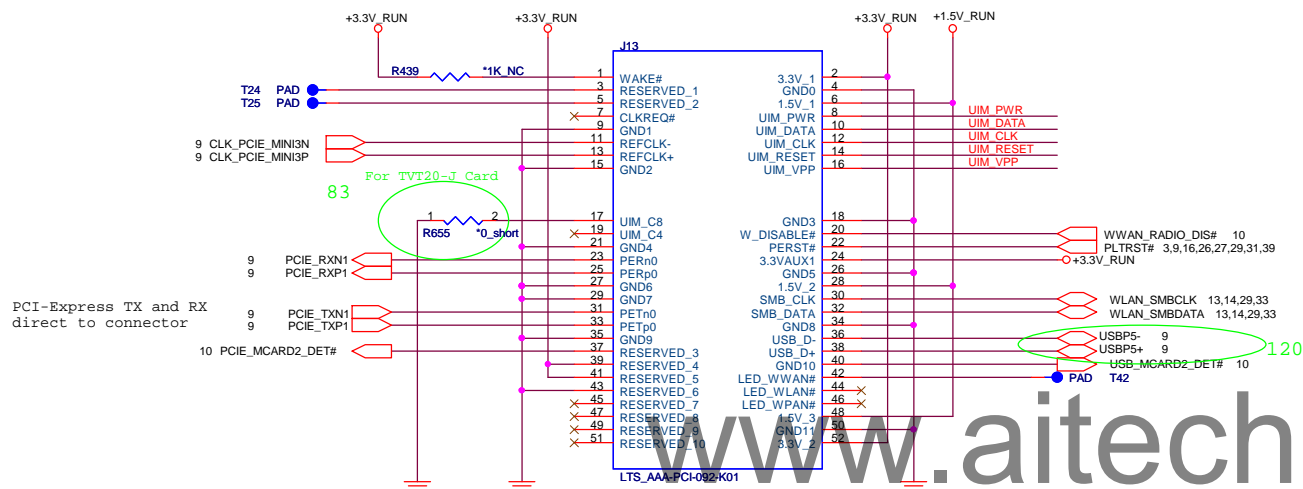
55
81
120

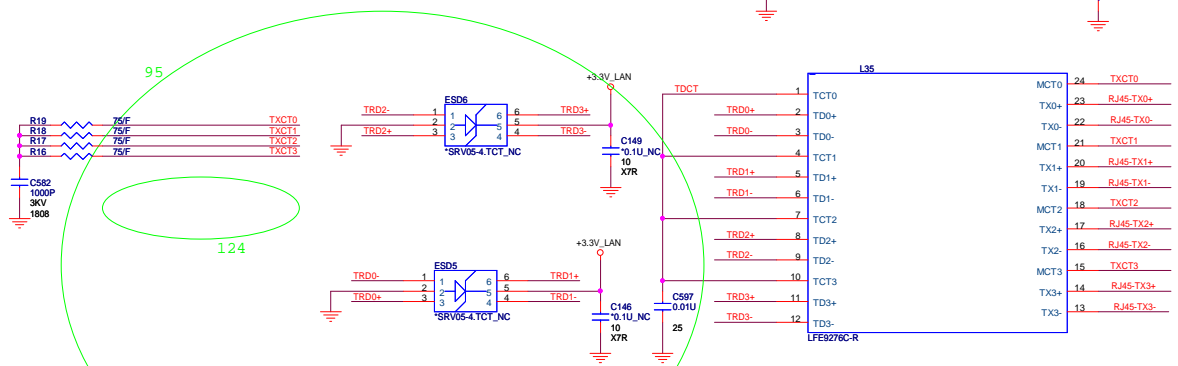
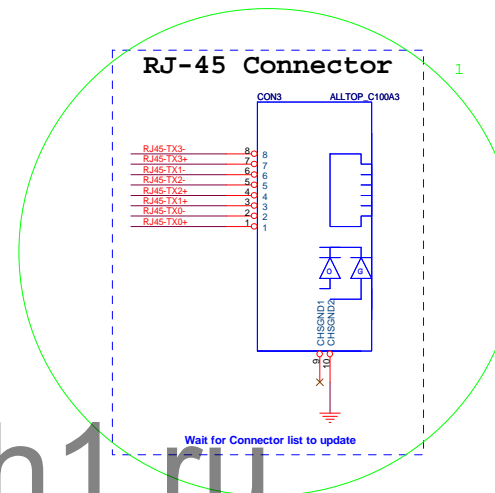
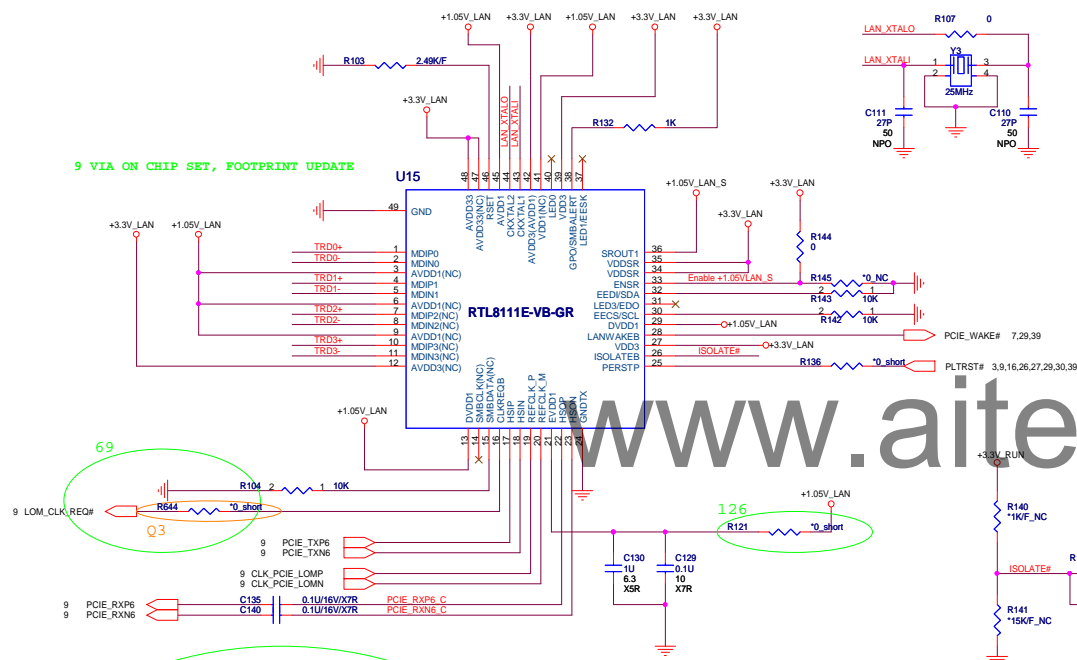
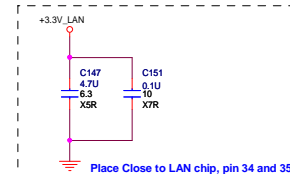
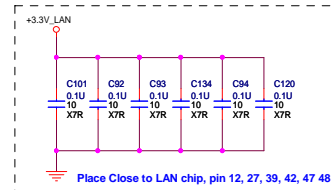
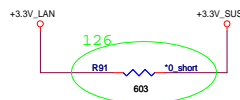


59

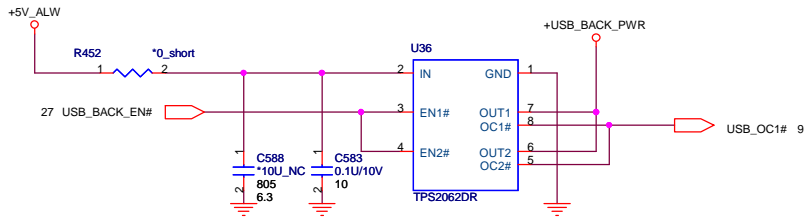


MiniCard WWAN connector

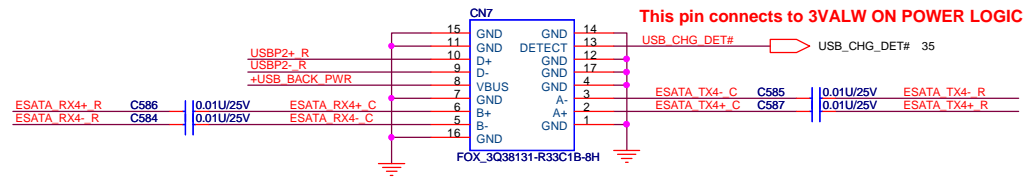
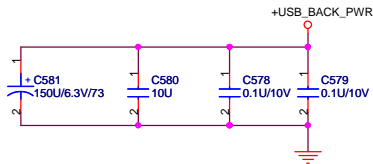




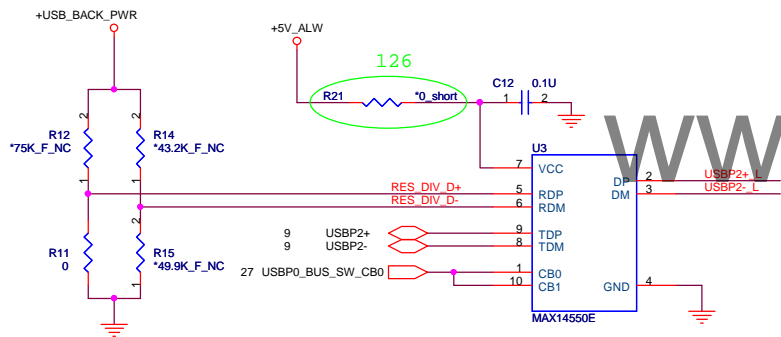
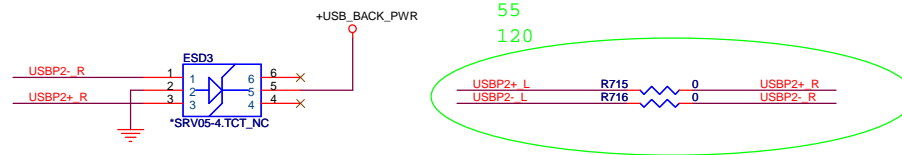
ESATA + USB Conn + Power Share



USB_BACK_EN# needs to be low when system S3 and S5 for USB charge



This pin connects to 3VALW ON POWER LOGIC



EC needs to drive CB0/CB1 pins to low when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

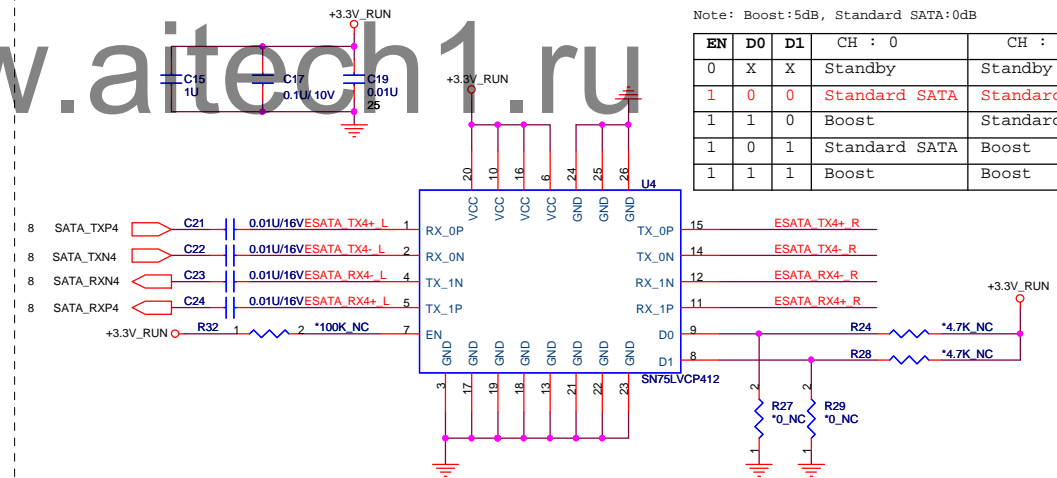
R15 needs to be 49.9K_F if we use external resistors.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
 (5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB

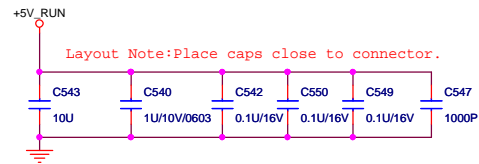
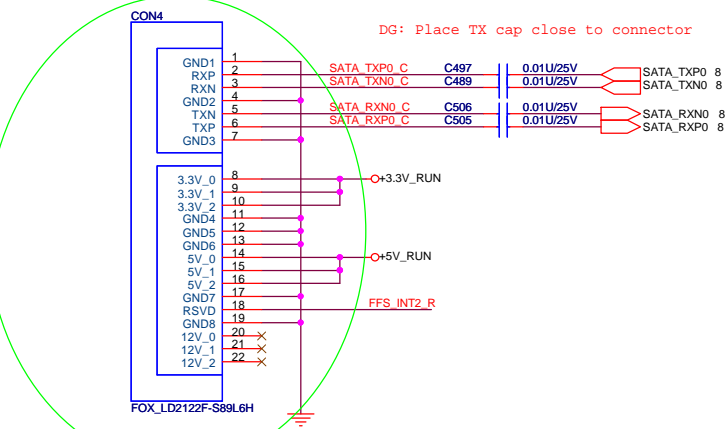


Note: Boost:5dB, Standard SATA:0dB

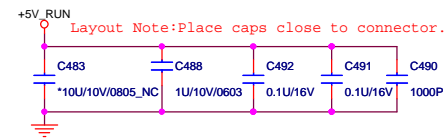
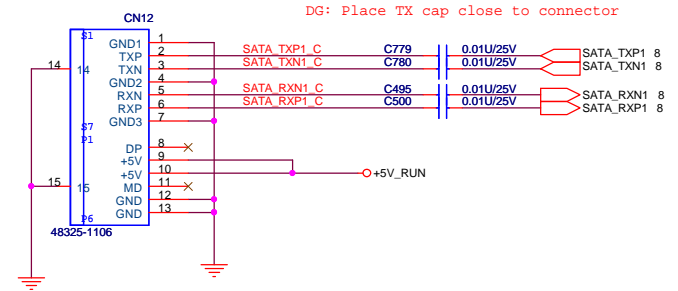
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

SATA Connector.

60

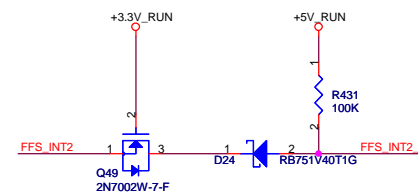
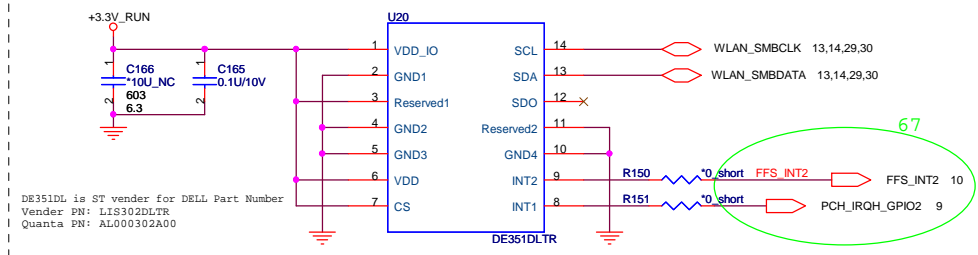


ODD Connector



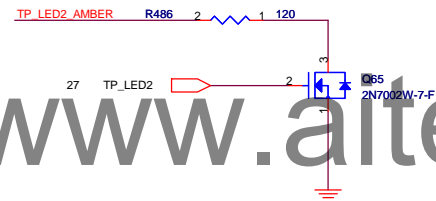
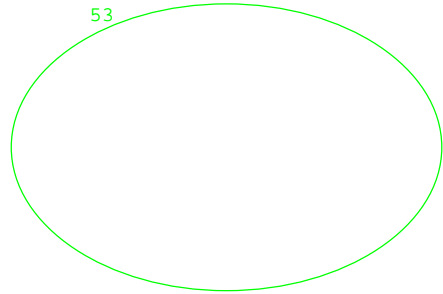
www.aitech1.ru

3-axis Fall Sensor (HDD data protector)

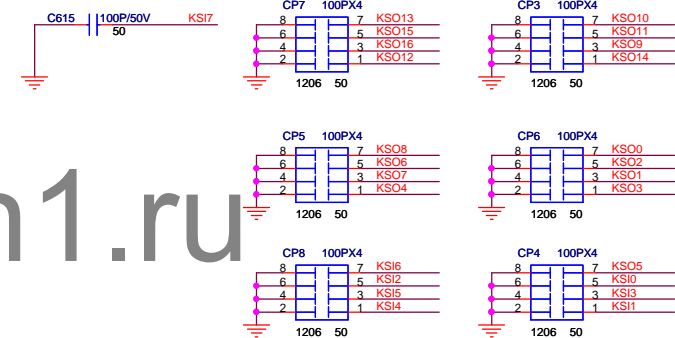
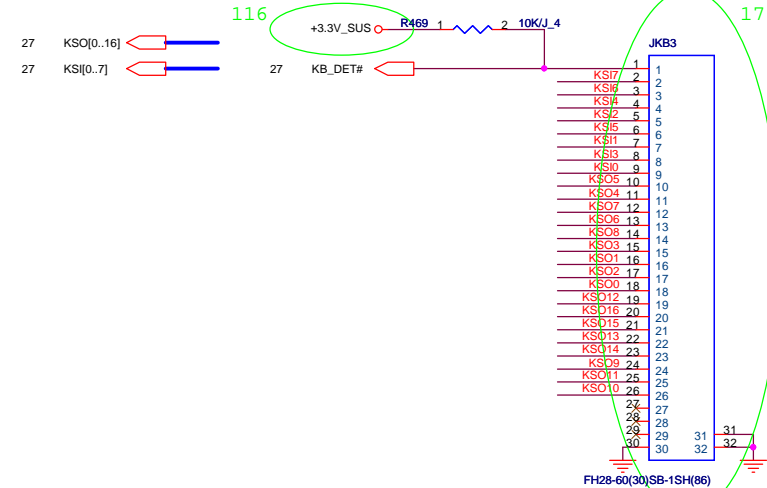


Title		
SATA (HDD&CD_ROM)		
Size	Document Number	Rev
GM6B		3A
Date:	Wednesday, September 01, 2010	Sheet 33 of 66

ON:White light on
OFF:Amber light on

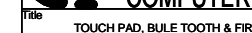
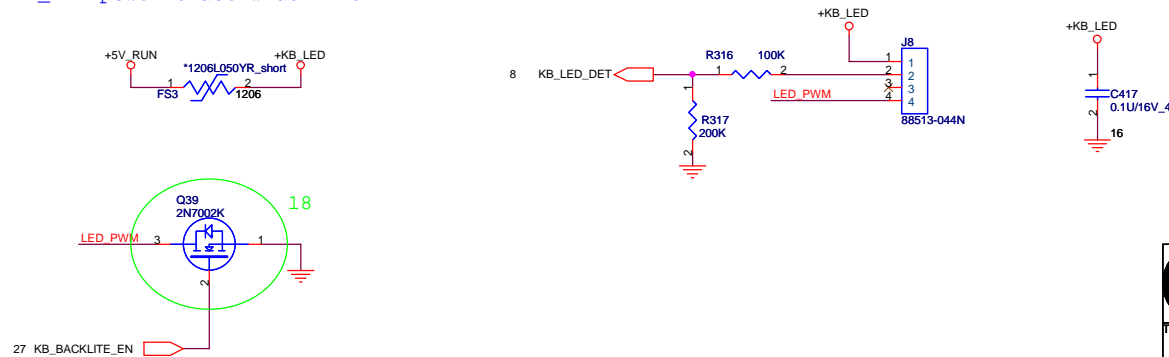


116



27 TP_LED2 2 Q65 2N7002W-7-F

```
+KB_LED power trace width >10 mil
```

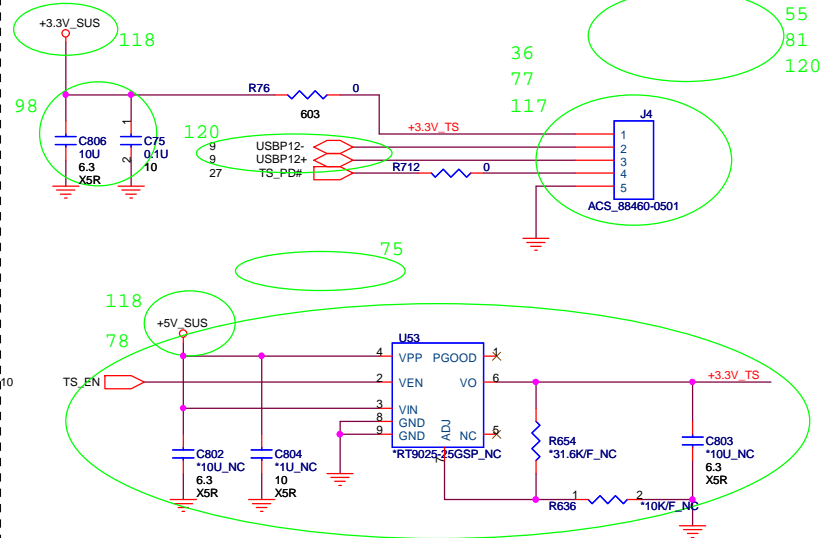


e	Document Number
---	-----------------

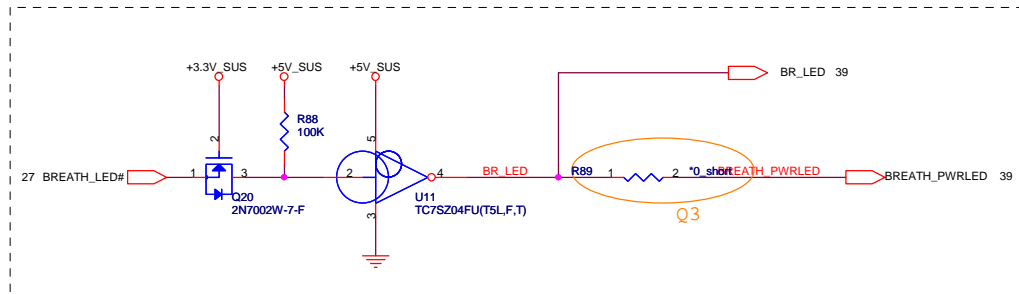
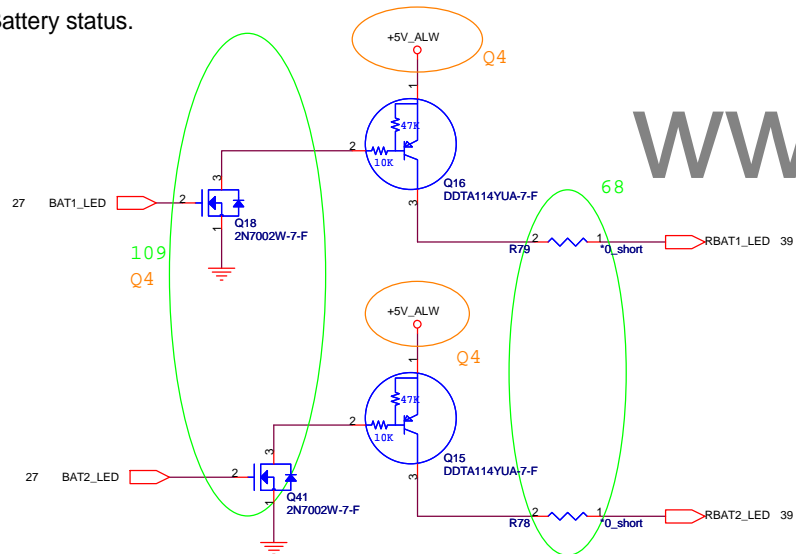
GM6B

Date: Saturday, August 28, 2010 Sheet 34 of 66

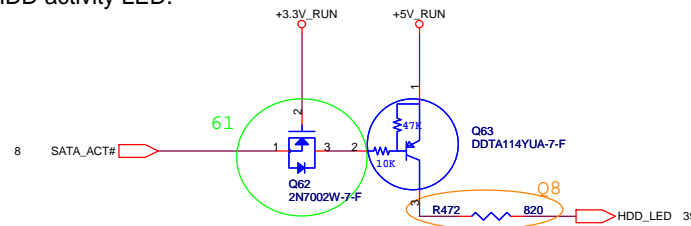
Touch Screen Module



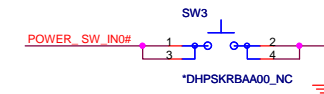
Battery status.



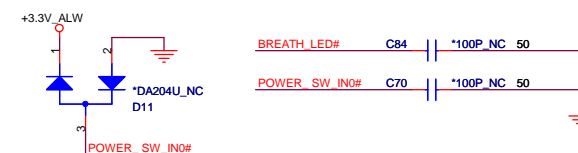
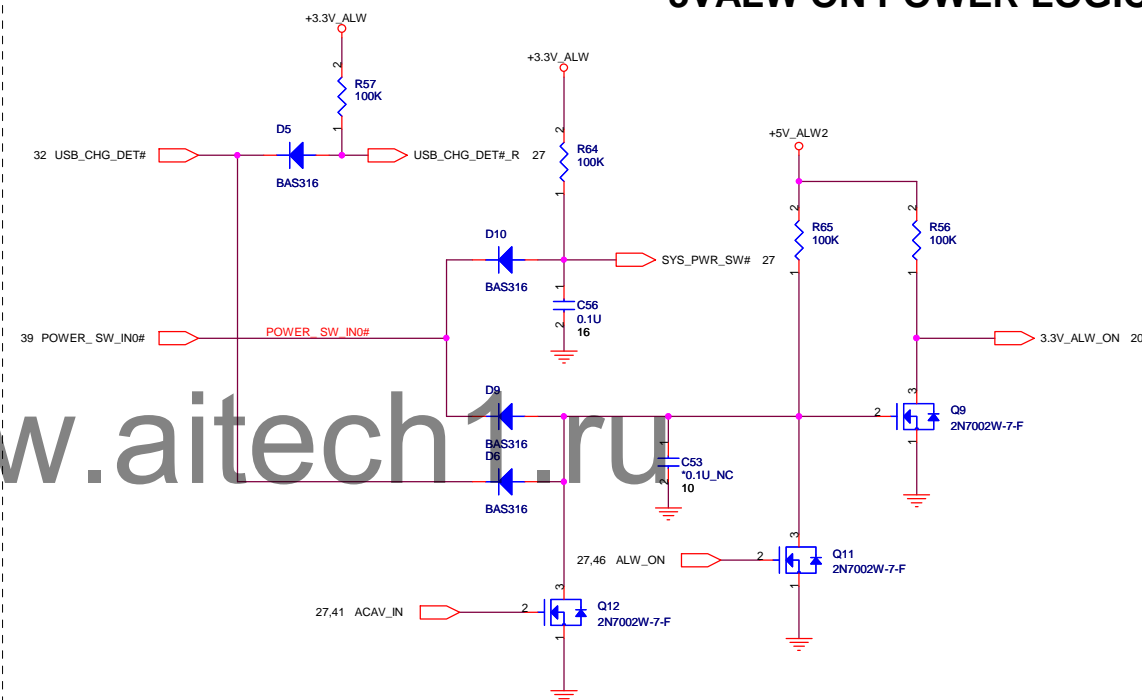
HDD activity LED.

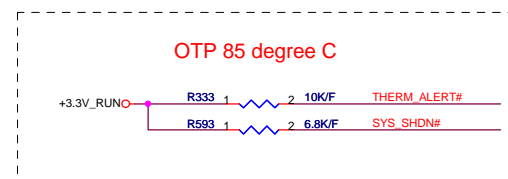
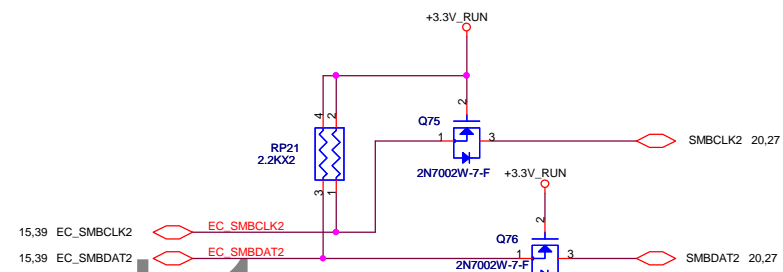
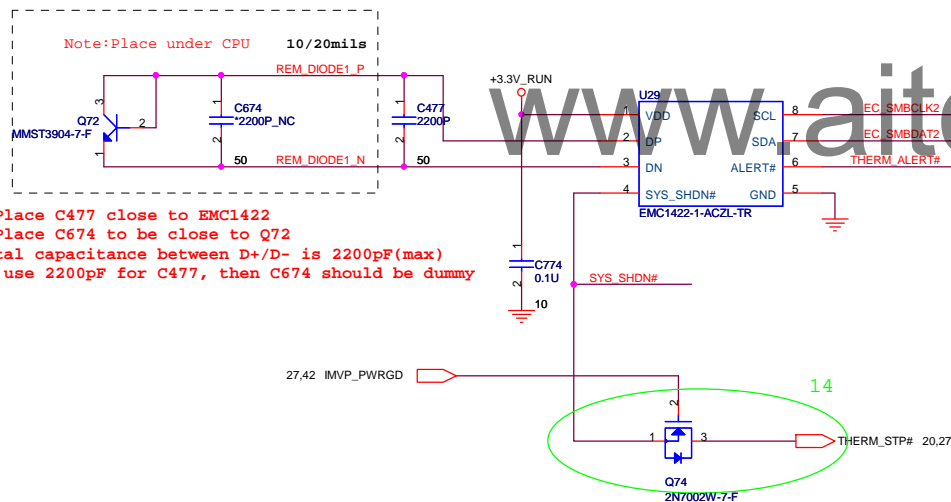
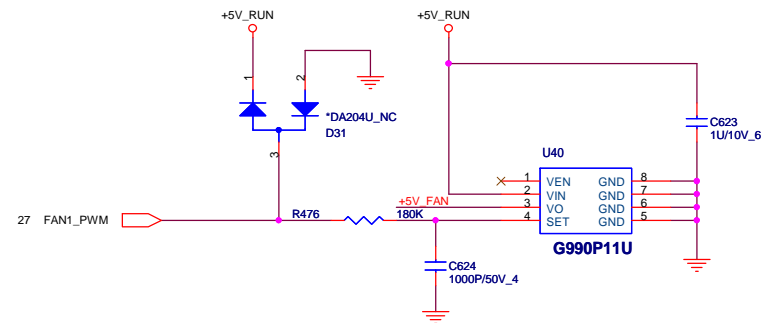
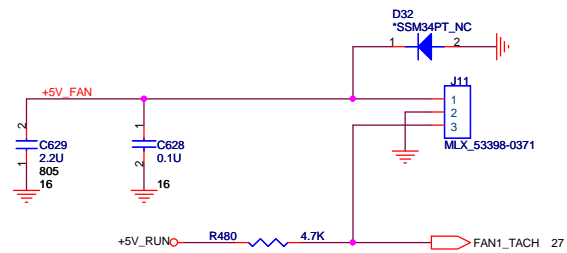


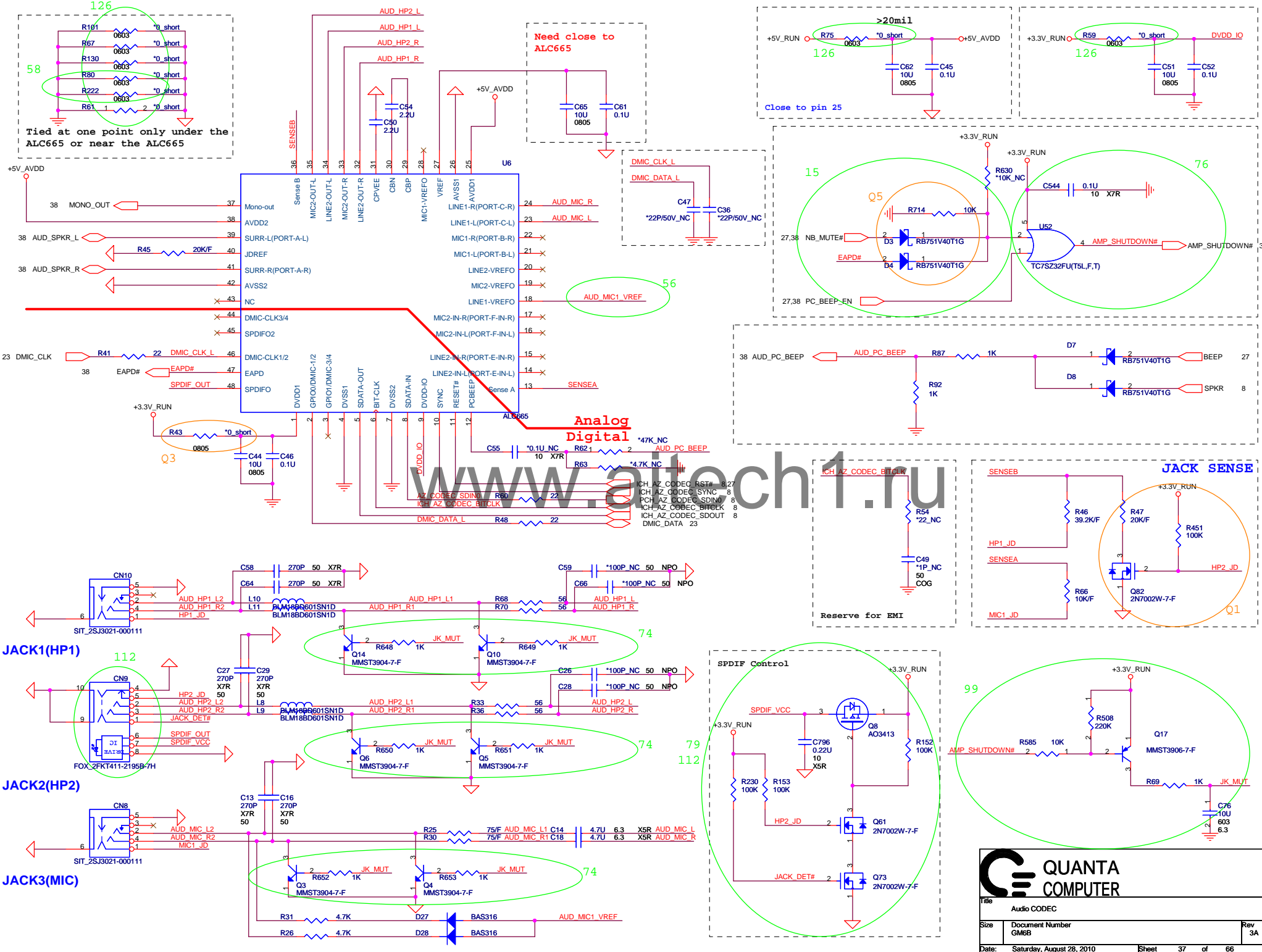
Power button for Engineer



3VALW ON POWER LOGIC

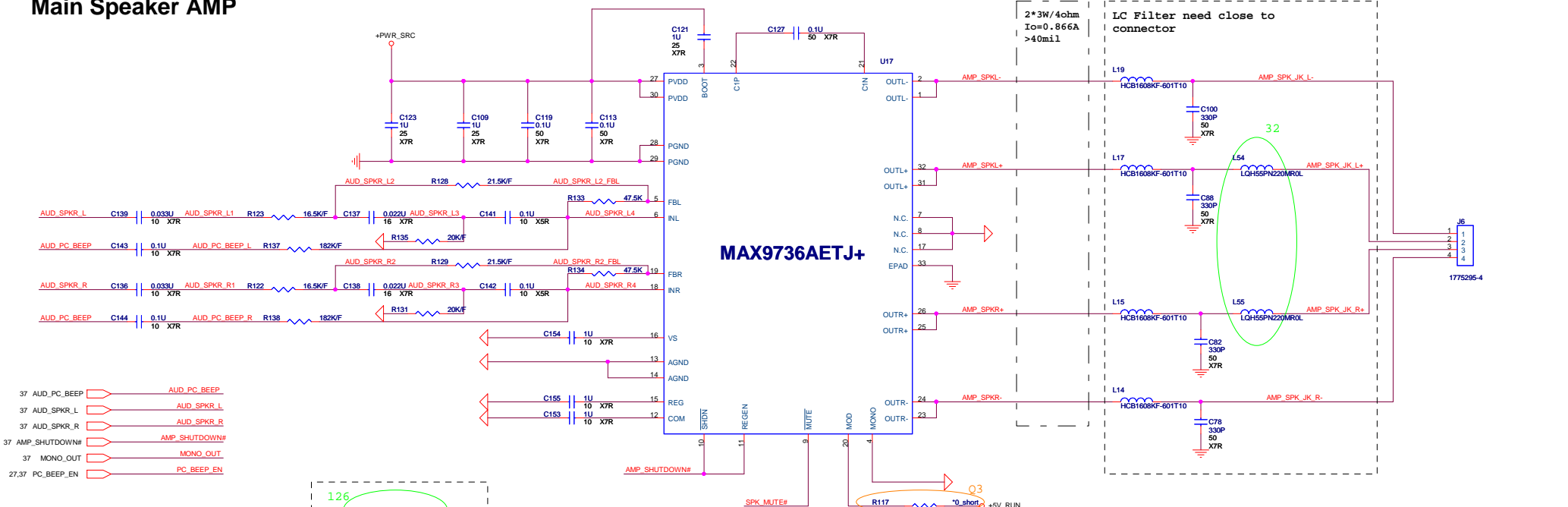




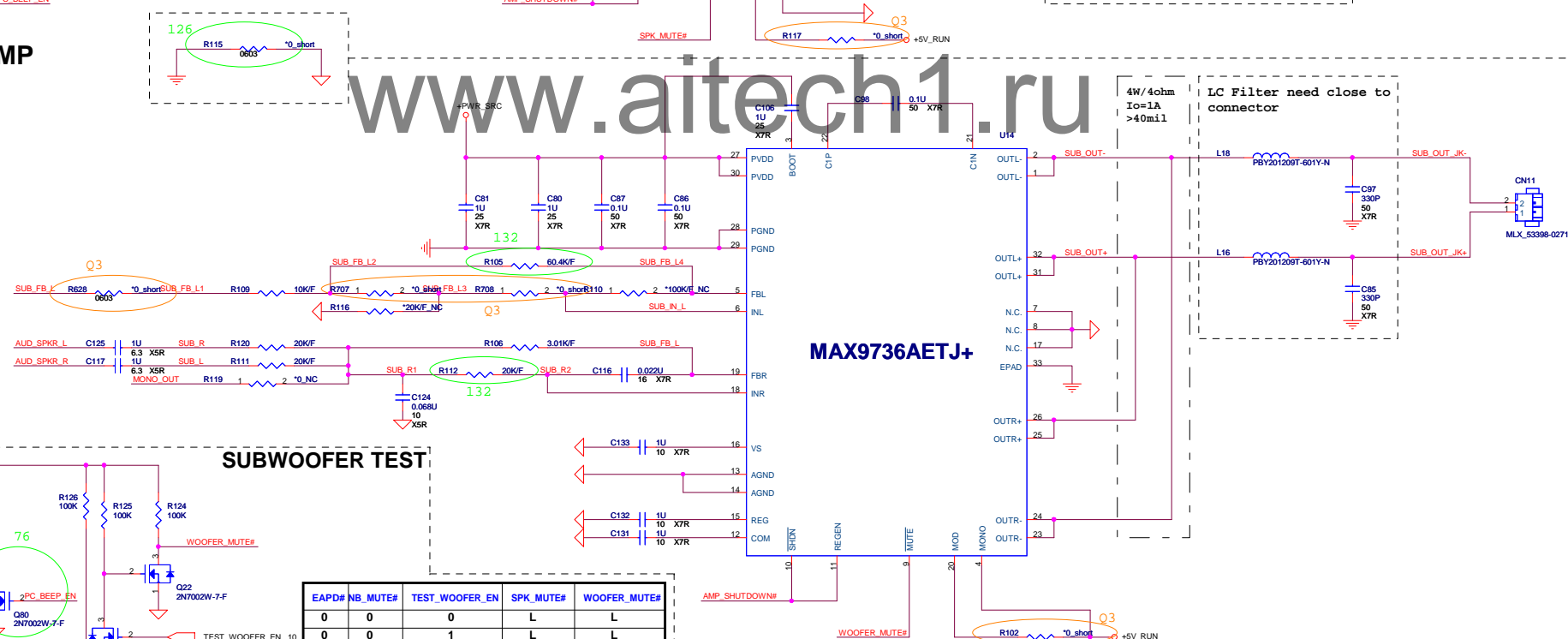


Title				Audio CODEC			
Size		Document Number GM6B				Rev 3A	
Date:		Saturday, August 28, 2010		Sheet		37 of 66	

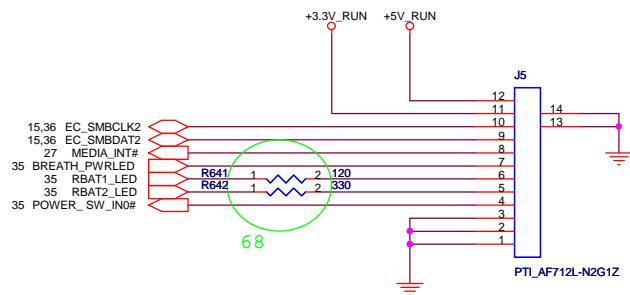
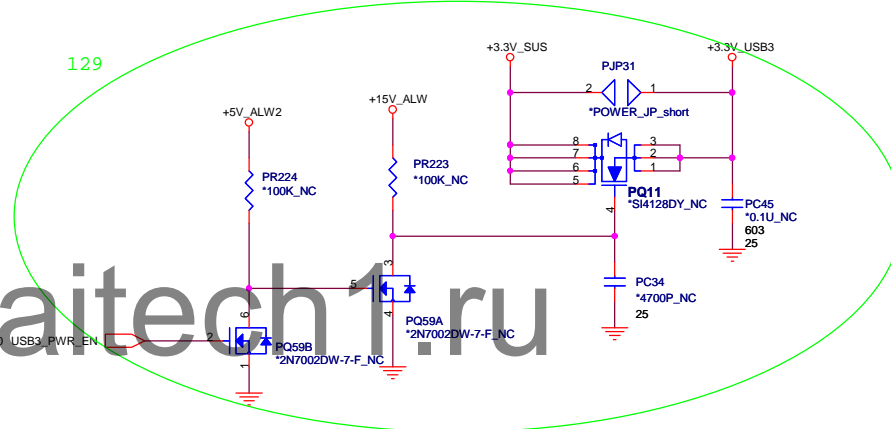
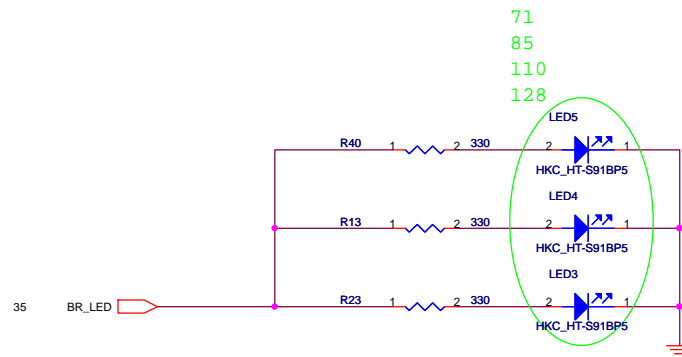
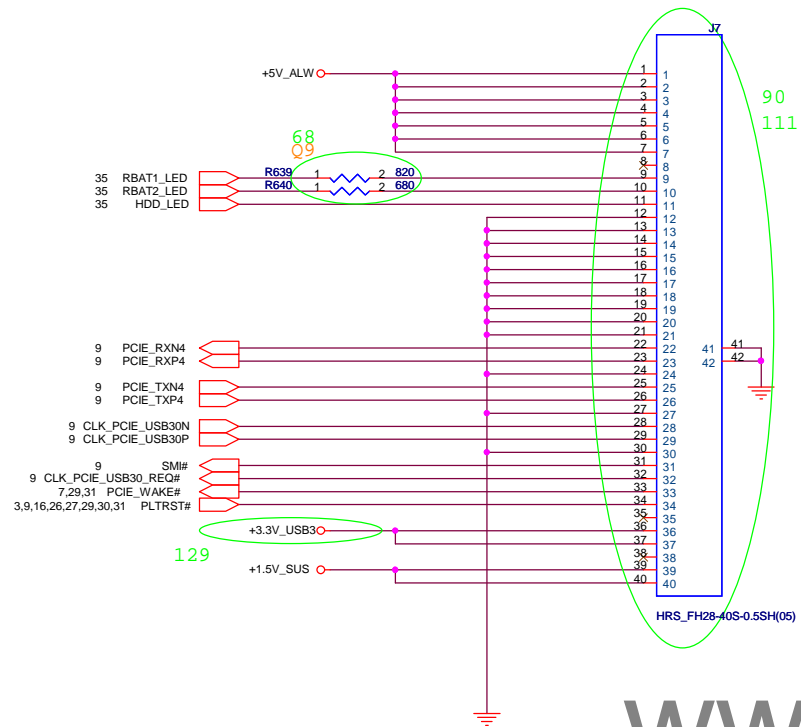
Main Speaker AMP

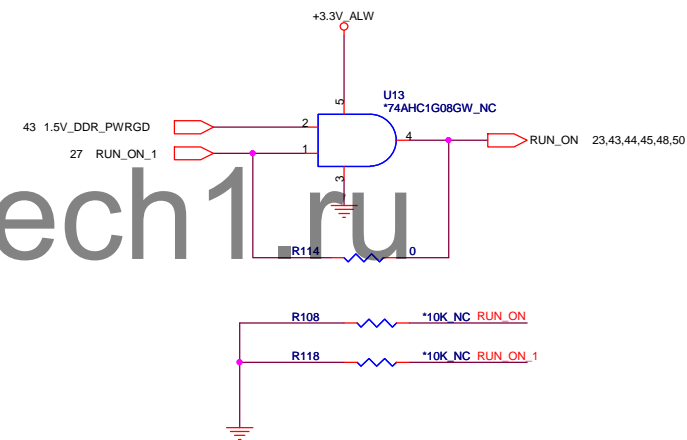
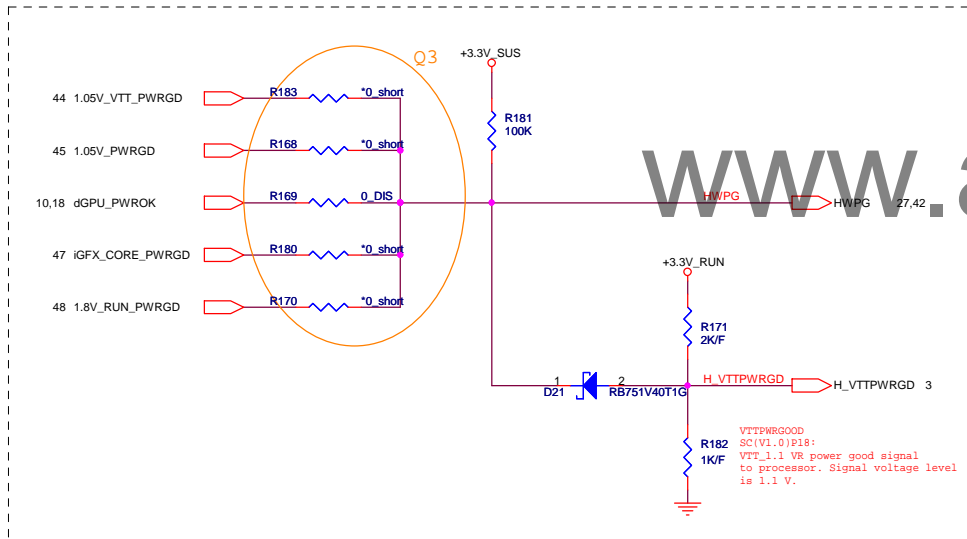
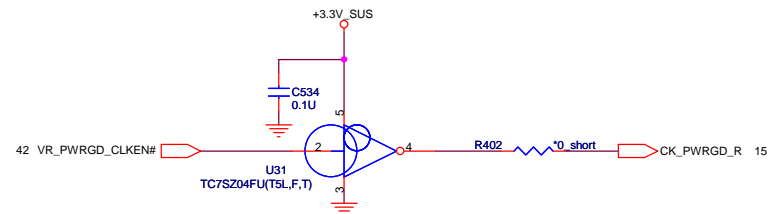


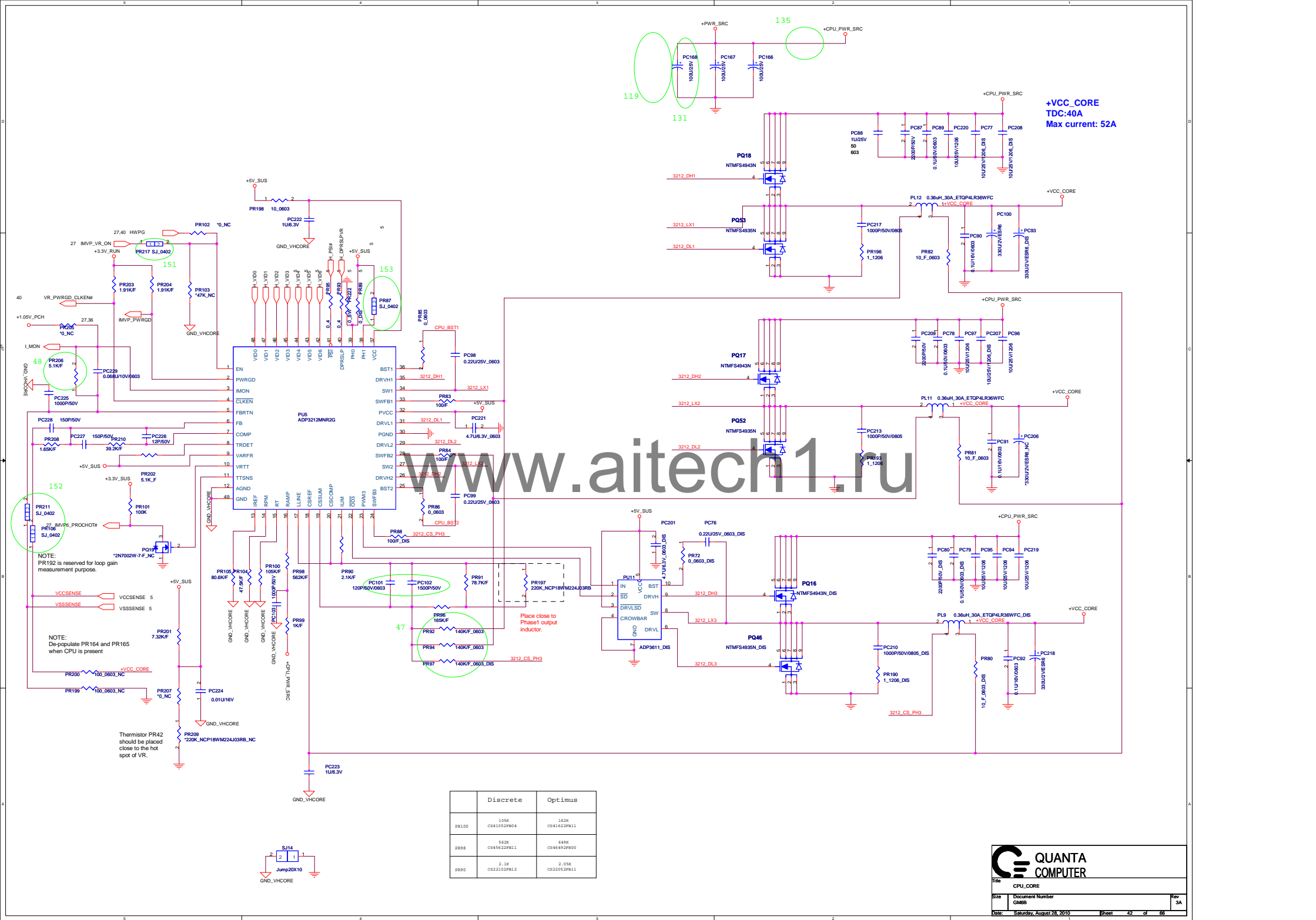
SUBWOOFER AMP

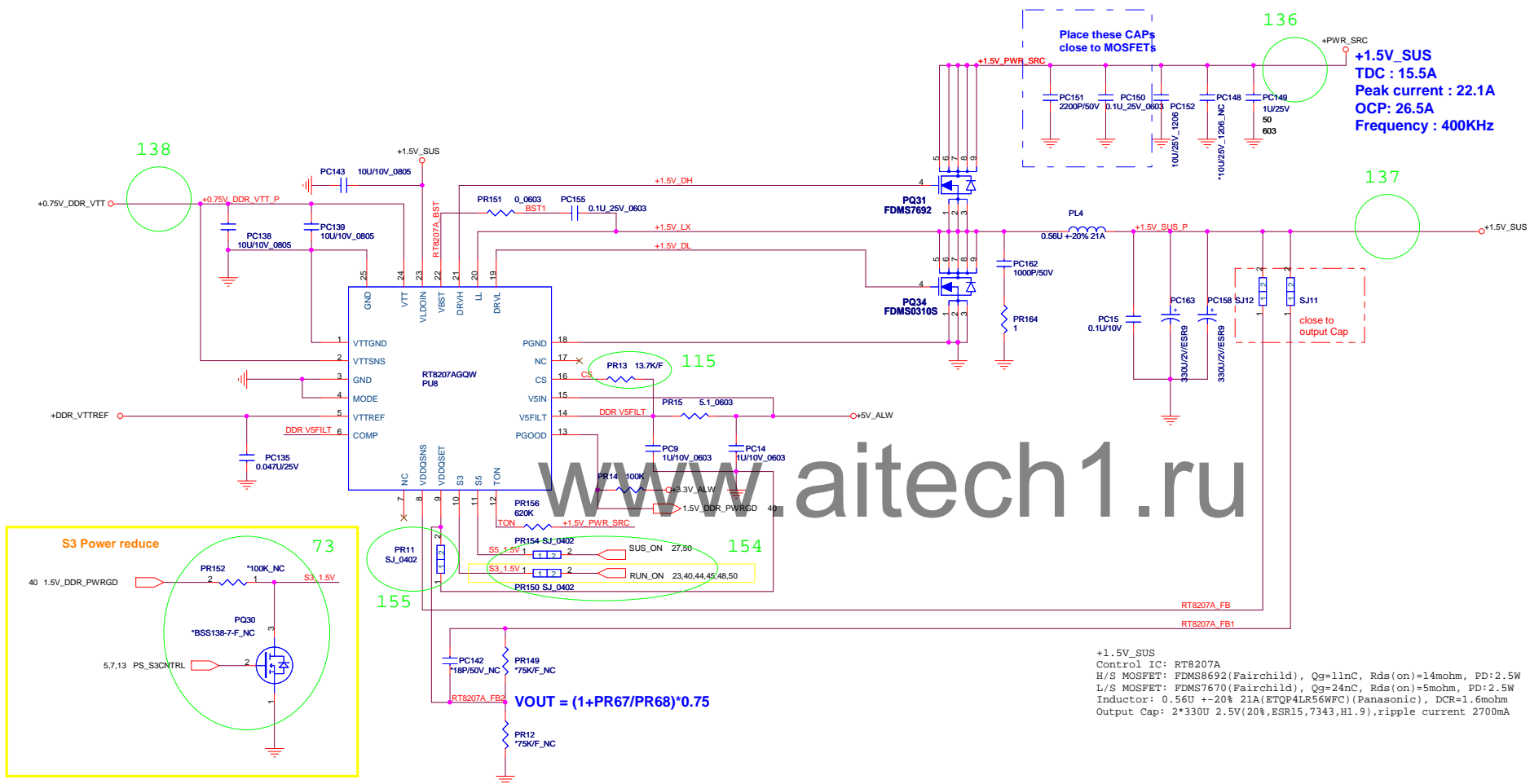


EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H









VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

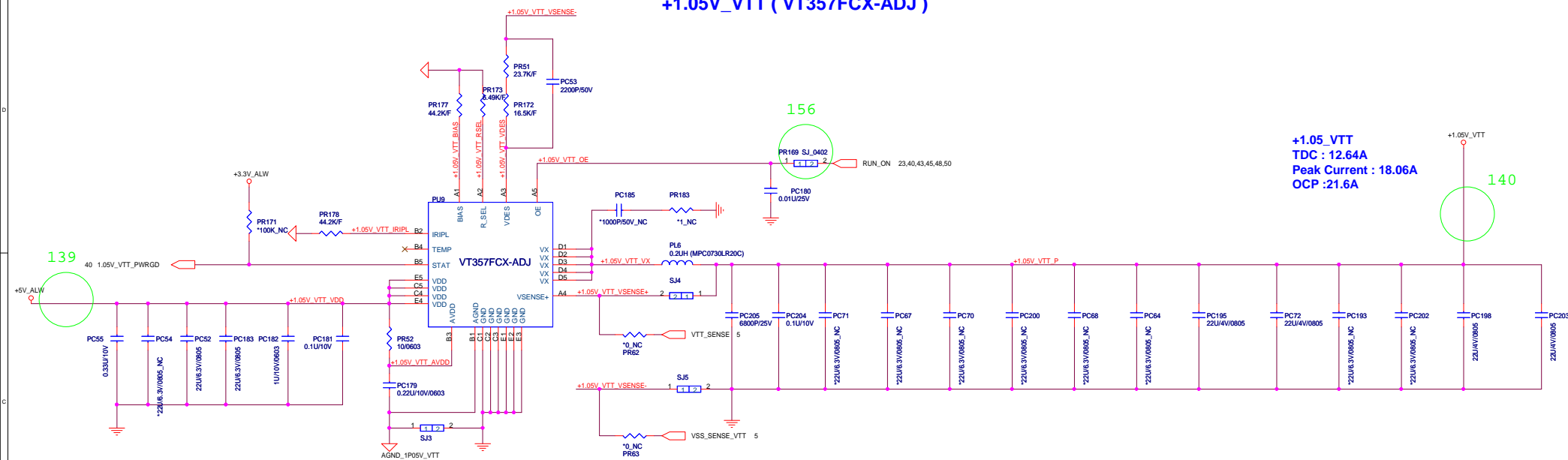
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

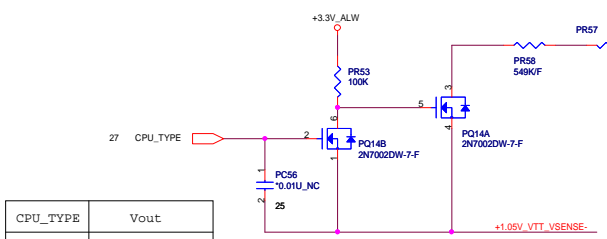
+1.05V_VTT (VT357FCX-ADJ)



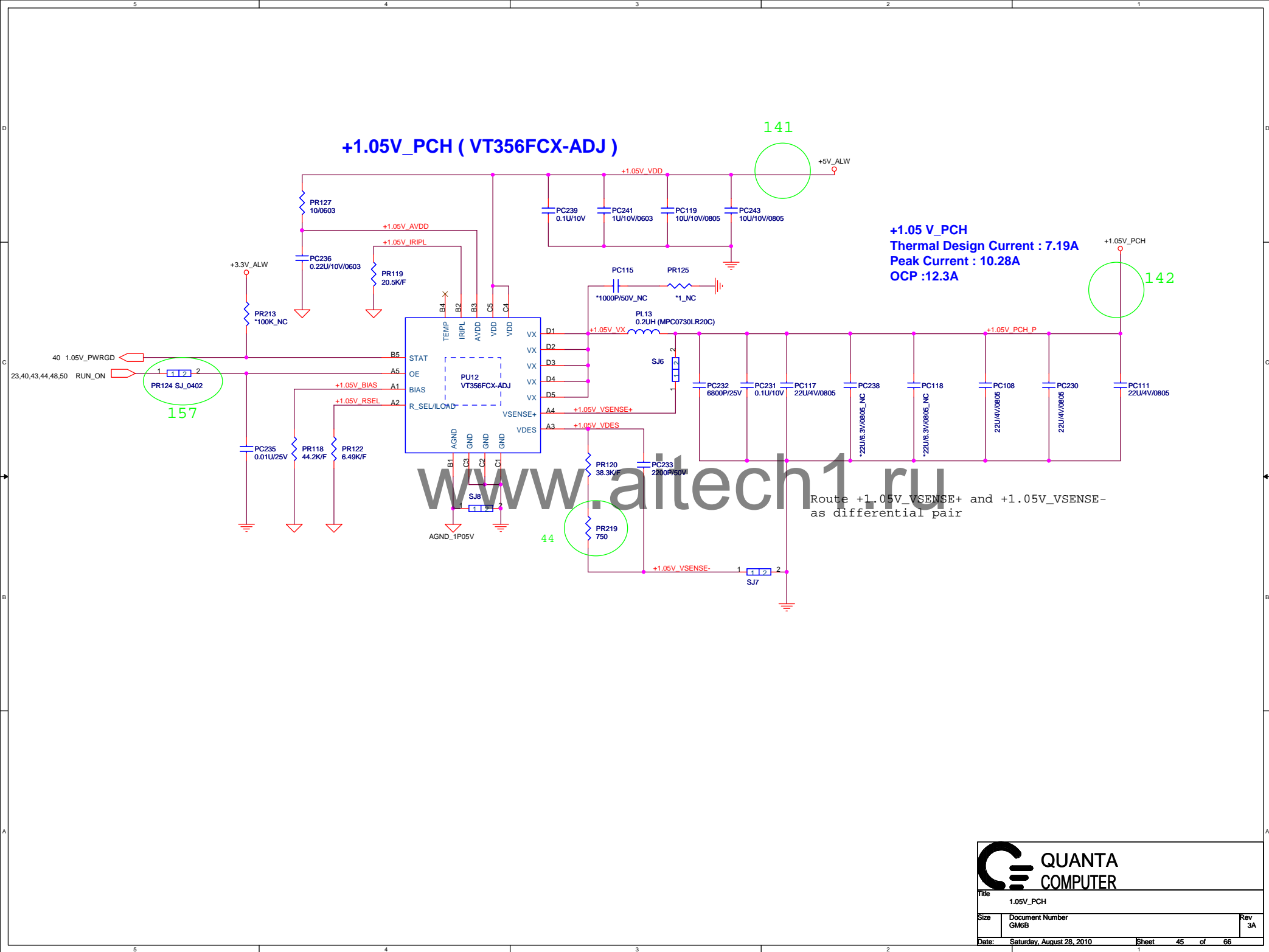
+1.05V_VTT
TDC : 12.64A
Peak Current : 18.06A
OCP : 21.6A

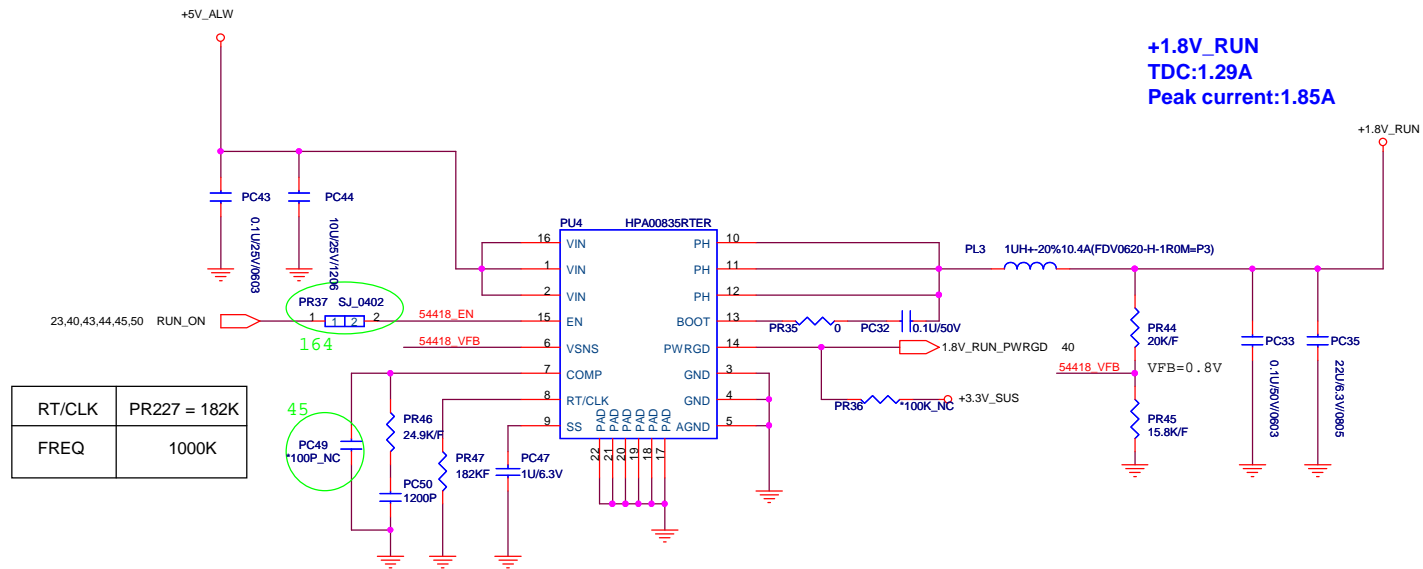
Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE- as differential pair

www.aitech1.ru

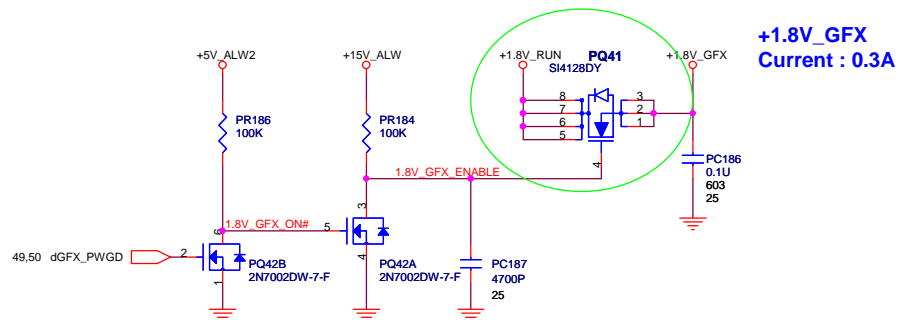


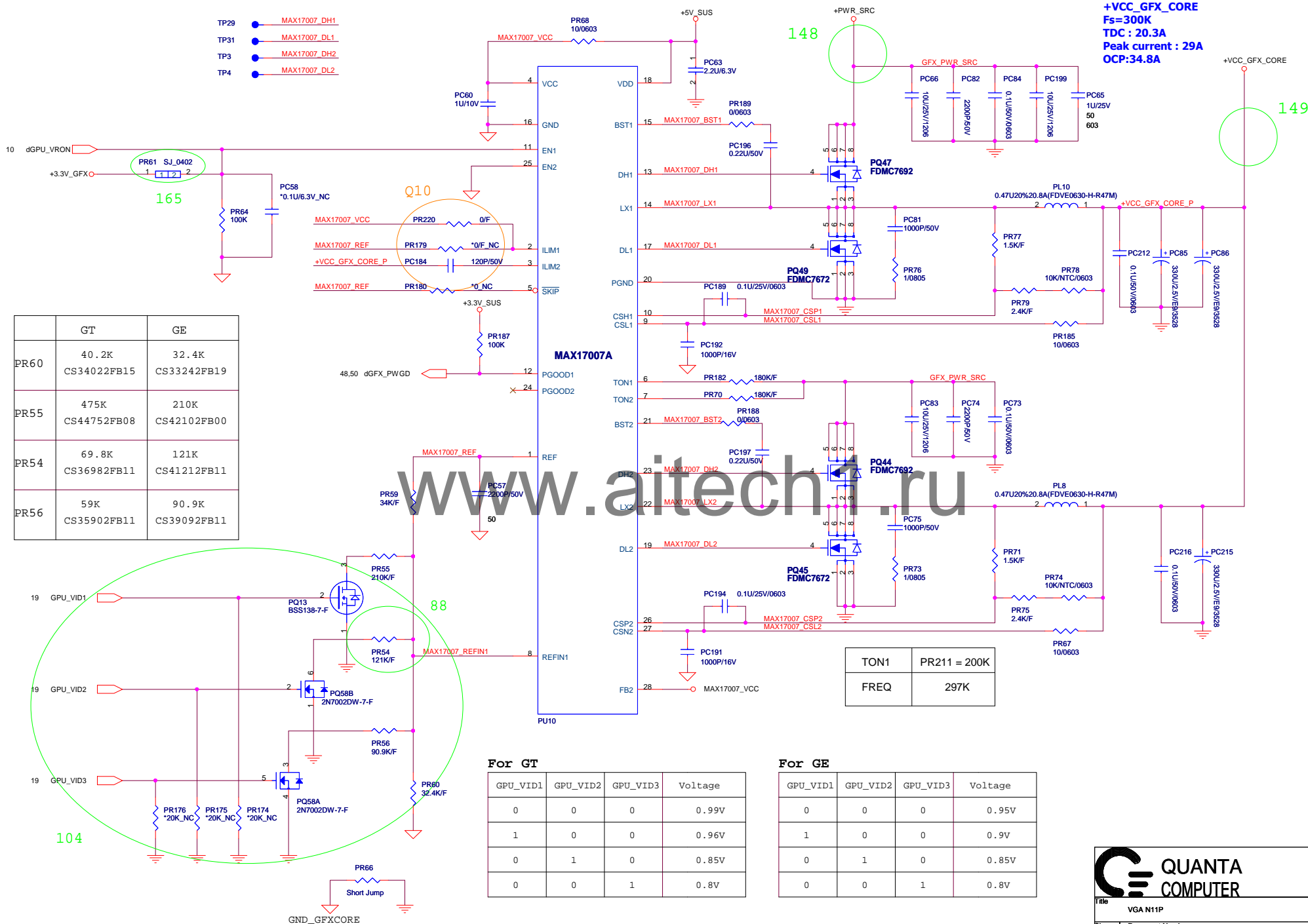
CPU_TYPE	Vout
L	1.05V(ARD)
H	1.1V(CFD)

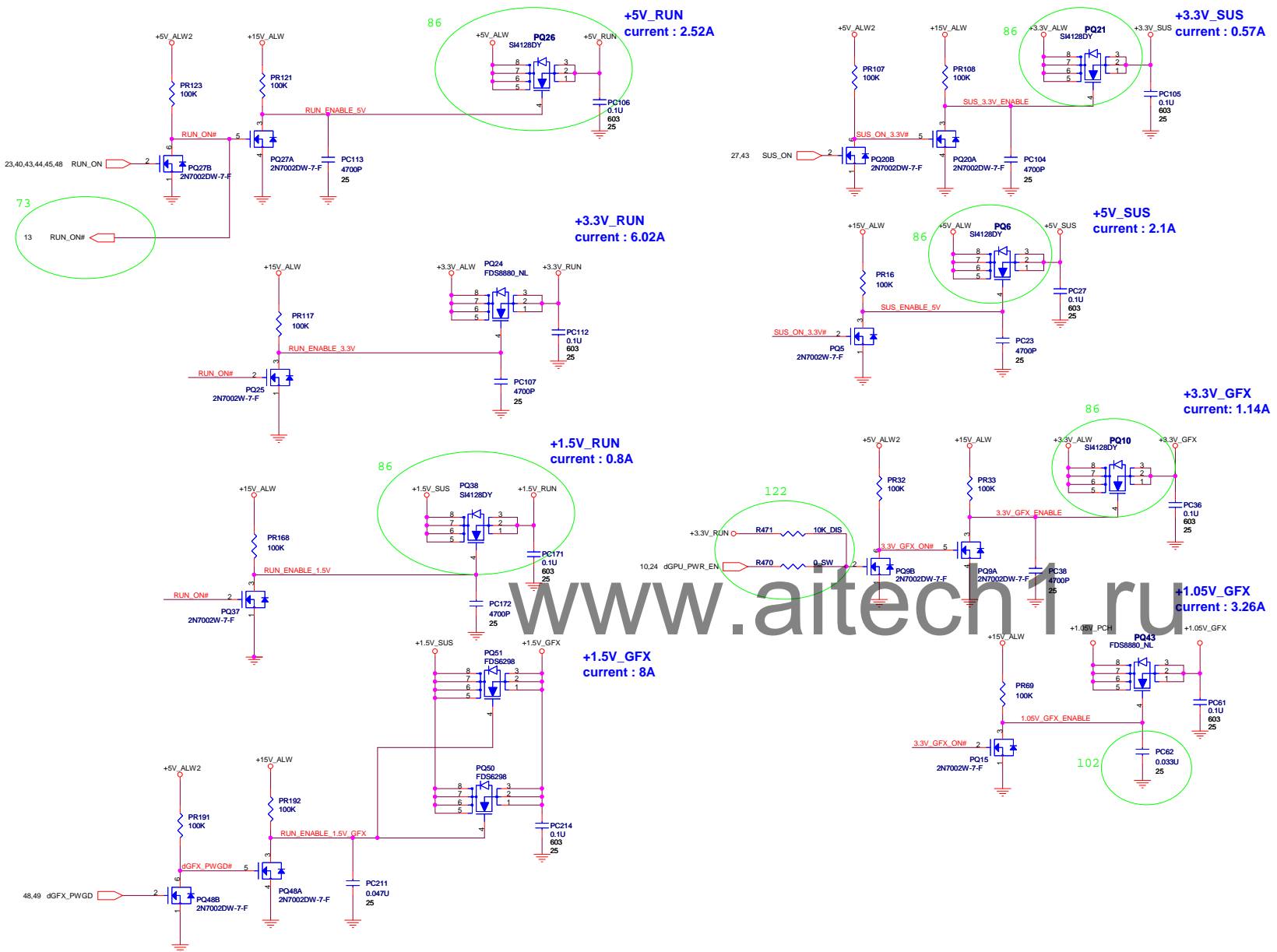


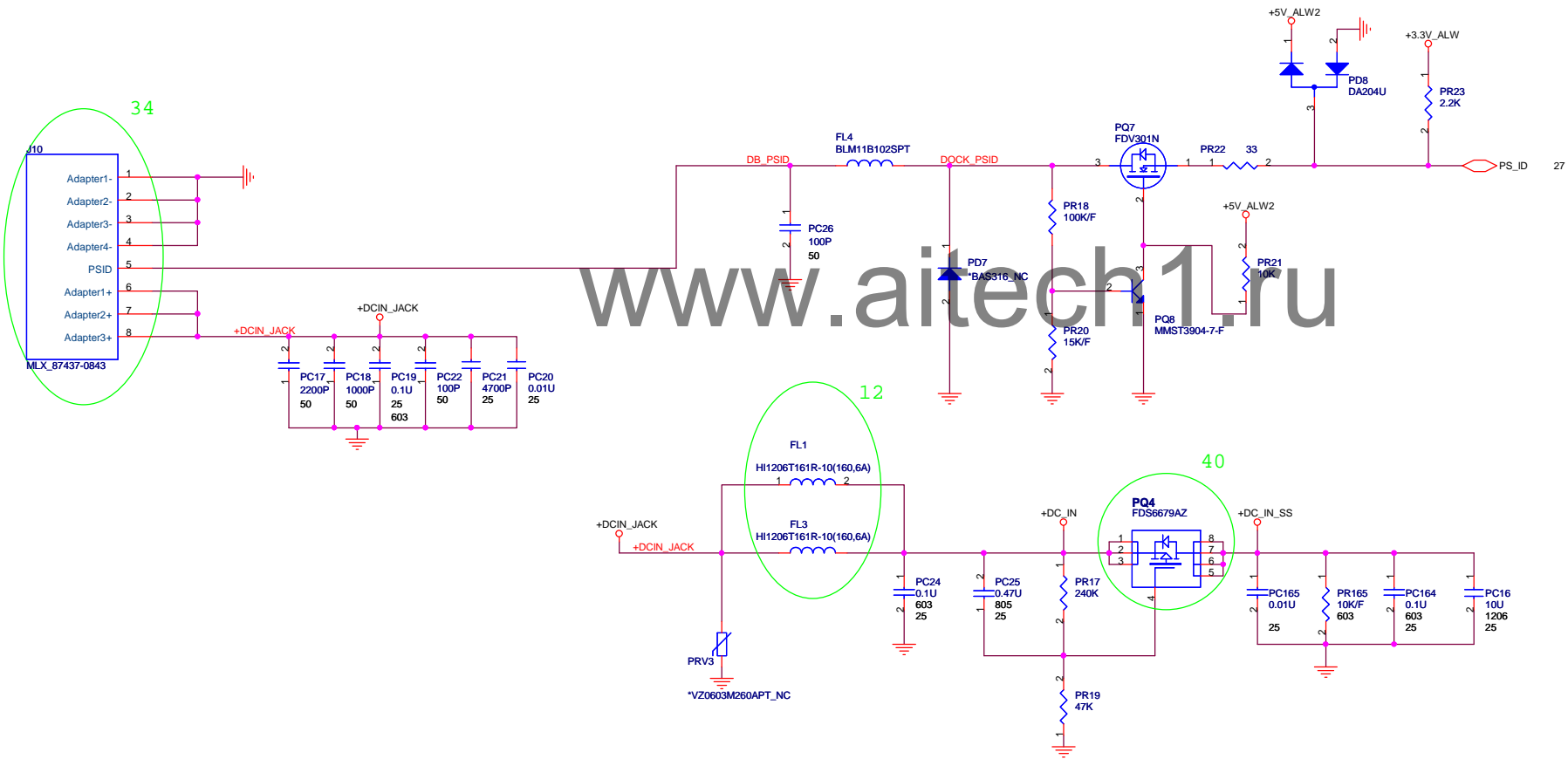
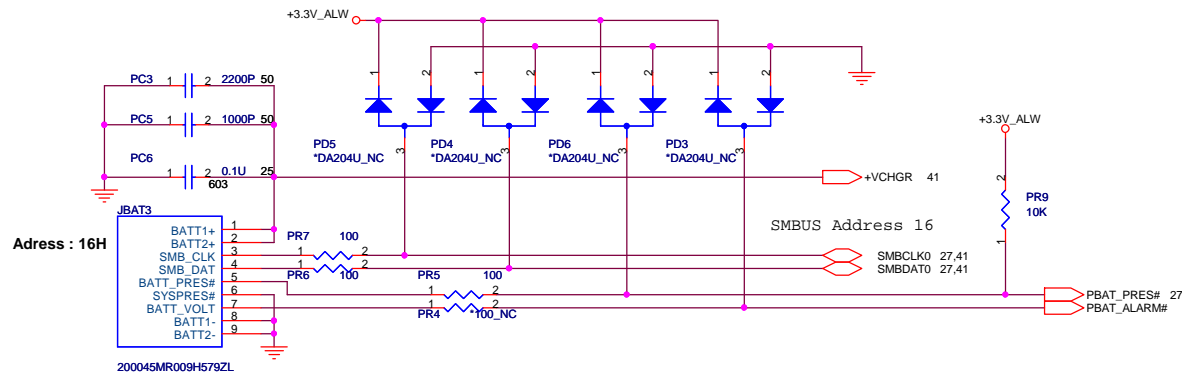


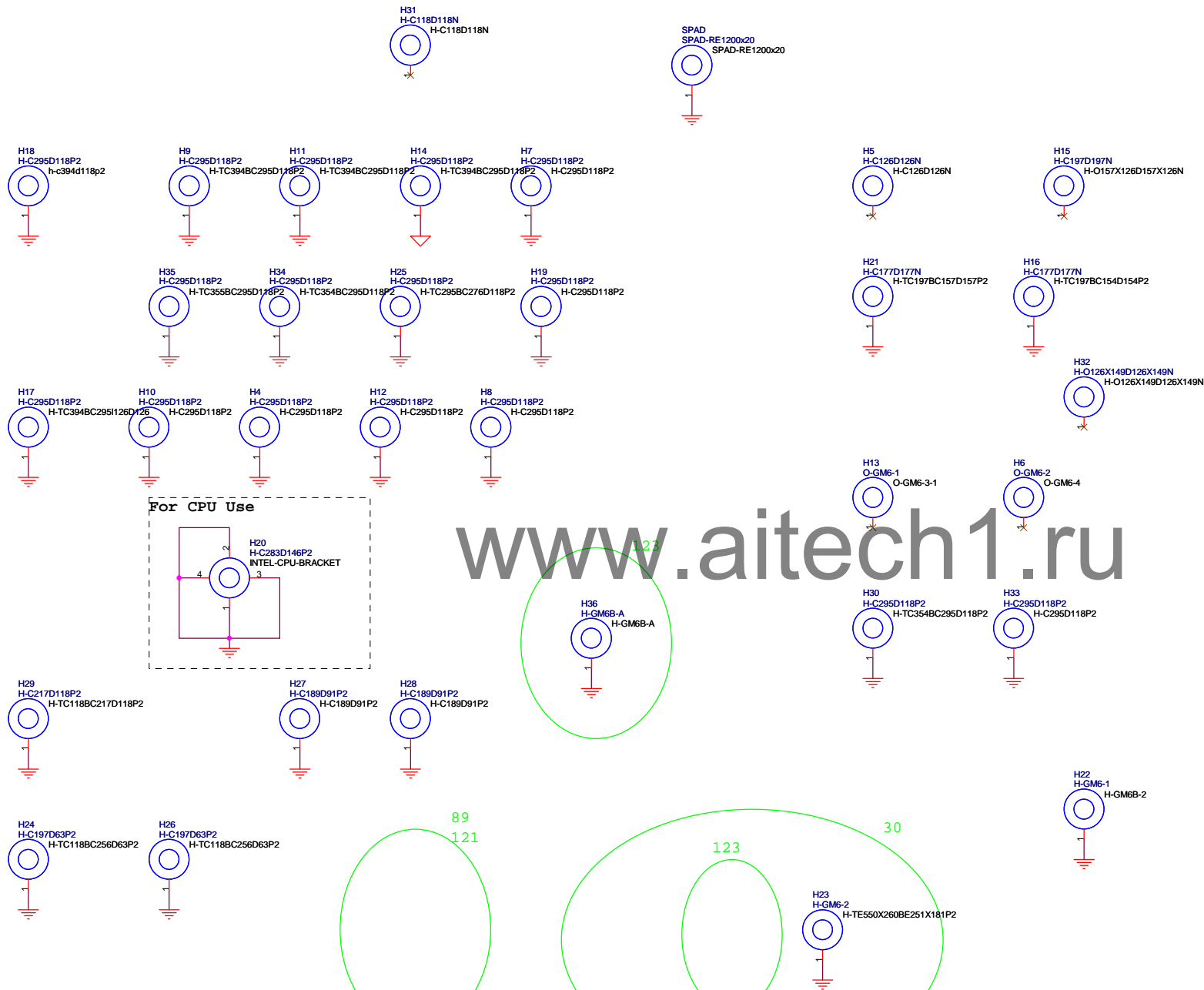
www.aitech1.ru





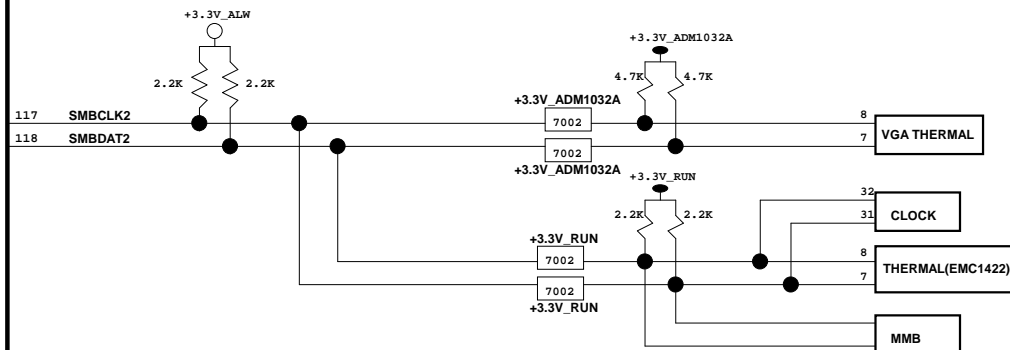
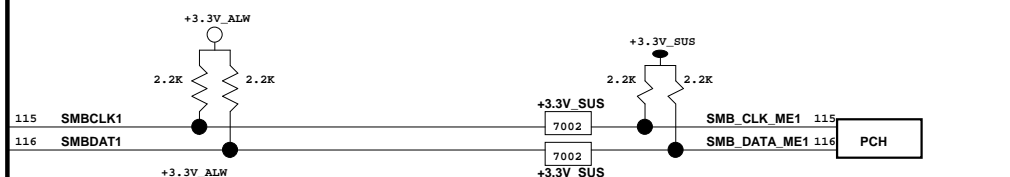
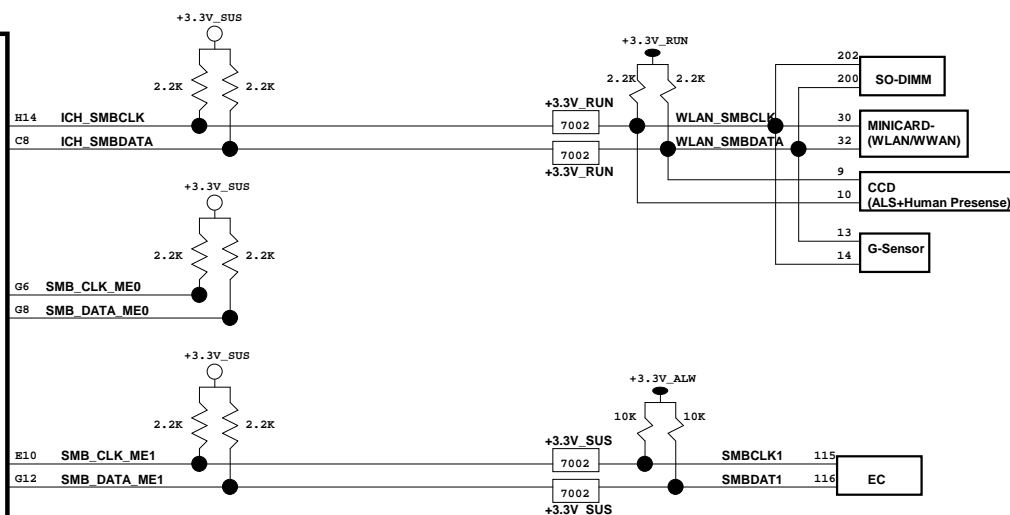


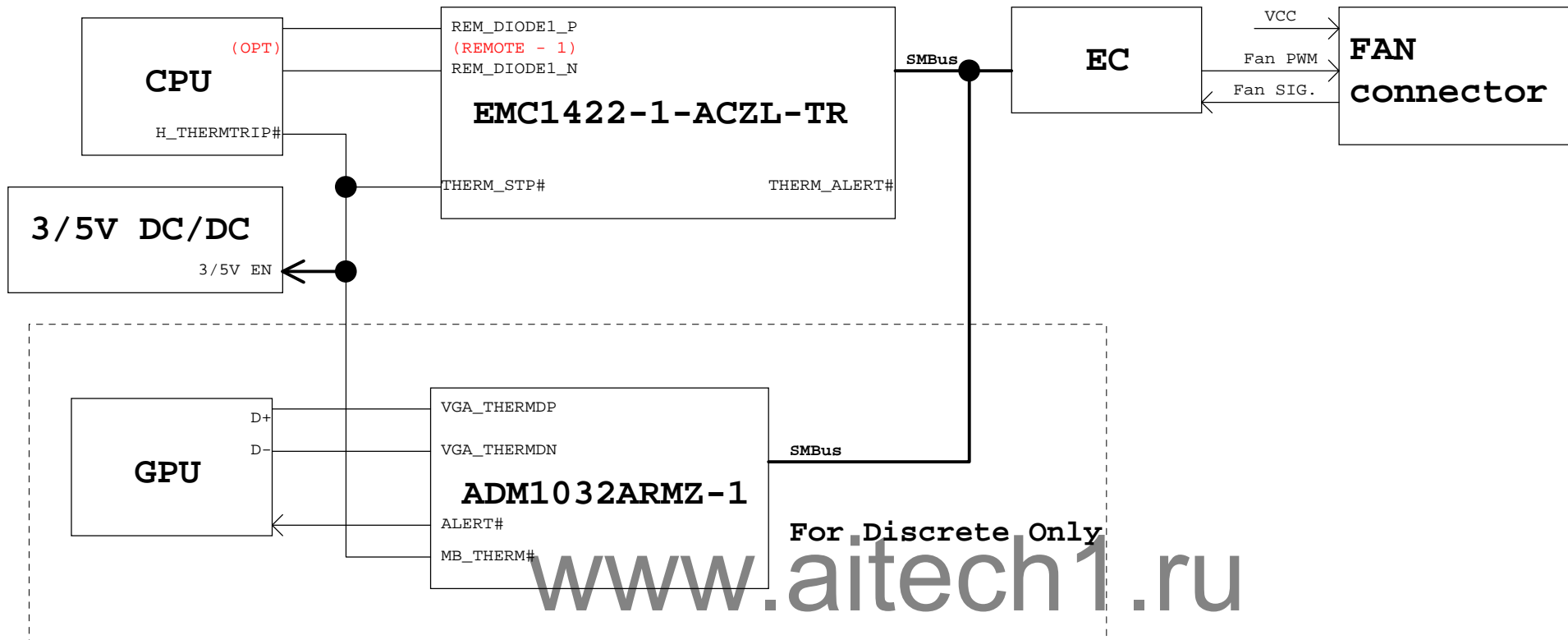


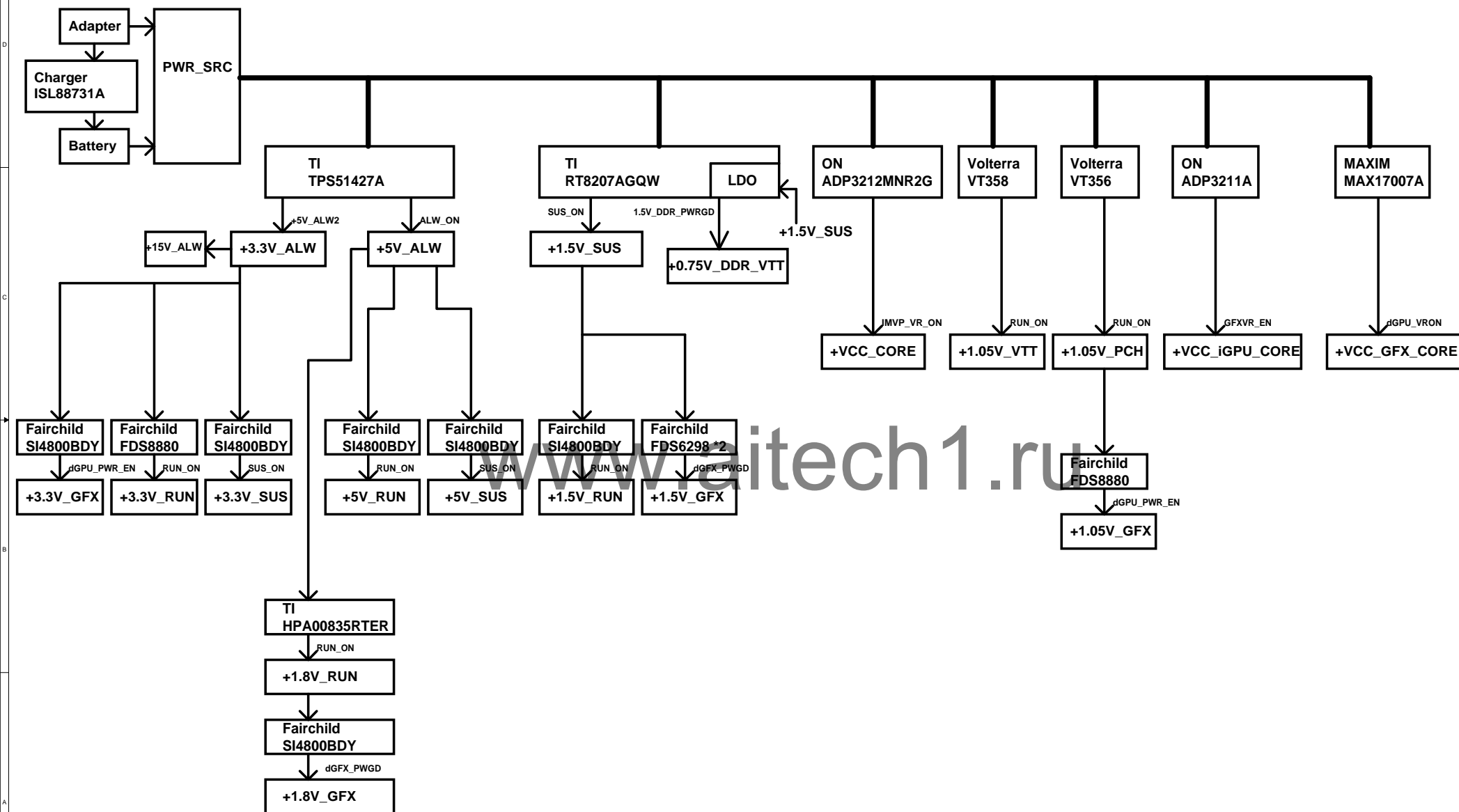


PCH

SIO
ITE8502







FM9 Power Design Block Diagram 2009/12/28

